# Characterization of Flip-Flop Designs at Subthreshold Voltages

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***Abstract*—As transistor sizes scale down, there is an increase in the power dissipation of digital circuits due to leakage and increased density. Subthreshold operation has become an efficient approach to decrease both the static and dynamic power dissipation of a circuit. Specifically, we are interested in the subthreshold behavior of flip-flop designs. In this paper we characterize the performance and power aspects of three master-slave flip-flop designs at near- and sub-threshold voltages. By analyzing the Clk-Q delay, setup time, and average power of a flip-flop, we provide insight into the performance and power information that is useful for subthreshold designers.**

## I. Introduction

Flip-flops and latches are the fundamental building blocks of digital electronic systems. It is important to understand the timing properties and energy efficiency of a flip-flop before it is incorporated into a design. A designer should be aware of the tradeoffs between performance and power of different flip-flop designs and choose the flop that best fits their needs. For example, if performance is the primary concern of a system, a fast flip-flop with a small minimum setup time and Clk-Q delay should be used. On the other hand, if power is the primary concern, a more energy efficient flip-flop design should be utilized.

As transistor technology scales down, there is an increase in the power dissipation due to faster switching (dynamic power) and increased leakage current (static power). An effective way of increasing the energy efficiency of a circuit is to operate the circuit at subthreshold voltages. As the supply voltage decreases, the leakage power decreases exponentially and dynamic power decreases quadratically. The major challenge of sub-threshold design, however, is that this same reduction in supply voltage exponentially decreases current and therefore increases delay. We can directly apply this to flip-flop designs which have been shown to operate at subthreshold voltages [1].

Certain aspects of a flip-flop must be considered during the design process; specifically it is important to know the Clk-Q delay, setup time, and hold time of a synchronous circuit. The reliability of a flip-flop is dependent on the setup time, or the amount of time that the input signal needs to be held constant before the clock event to ensure that the input is reliably sampled. A setup time violation can force the flip-flop into a meta-stable state where the output signal becomes unstable or the propagation (Clk-Q) delay is significantly increased. Also, the sum of the setup time and the Clk-Q delay directly influence the amount of time consumed by the flip-flops. In heavily pipelined designs, the overhead of the flip-flops can be significant. Last, the hold time of a flip-flop often requires extra time padding to enable the reliable capture of signals. It is important to note that at lower supply voltages, an increase in delay, setup time, and hold time is expected, however, the ratio at which these scale for different flip-flop implementations is important for designers to consider.

Previous works [2], [3], have analyzed and compared the propagation delay, minimum setup time, and average power dissipation of various flip-flop designs at subthreshold voltages, but the authors provide minimal information regarding the methodologies used to determine the timing and power characteristics of a design. We propose a methodology to analyze a flip-flop design and provide the propagation delay, minimum setup time, and average power of the flop at both near- and sub-threshold supply voltages. The goal of this methodology is to outline the performance and power tradeoffs of specific flip-flop designs so that a designer can choose the appropriate flop. We also determine that a master-slave flop [3] is the most efficient in the subthreshold region, with another design [4] having similar efficiency in the super-threshold region. To our knowledge, some of these designs [4] have not been analyzed using sub-threshold supply voltages.

Our work proceeds as follows: Section II explains how we perform the timing analysis on the flip-flop to obtain the Clk-Q delay and minimum setup time. Section III explains the method used to analyze the power dissipation. Section IV provides a description of the simulation setup and the flip-flop designs used in the experiment. Finally, Section V outlines the results obtained.

## II. Timing Analysis

The timing analysis of a flip-flop circuit is performed using a Python script that automates the HSpice circuit simulation. The Python script first determines the Clk-Q delay of the flip-flop and then uses a bi-directional search to find the minimum setup time. The setup and Clk-Q delay are illustrated in Figure 1.

### A. Clk-Q Delay

The Clk-Q, or propagation delay, of a flip-flop is defined as the time elapsed between the clock signal and the output signal. The delay is measured using the points in time where

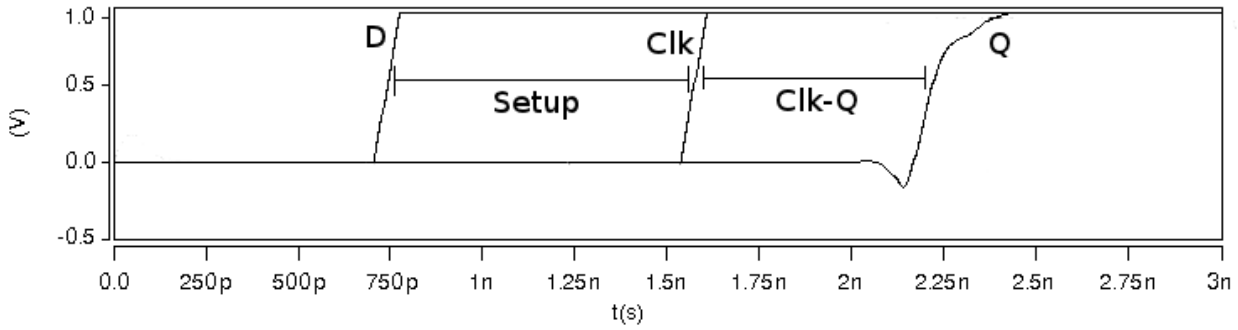


Fig. 1. The Clk-Q delay is the difference in time between the 50% points of the Clk and Q signals. The setup time is the time that the input is held steady before the clock event.

each signal reaches 50% of the supply voltage, as seen in Figure 1. Our Python script writes control statements into the spice netlist of a flip-flop and runs a Hspice transient simulation. We use a piecewise linear function for both the input and clock signals, set the desired supply voltage, and use a .measure statement to measure the delay. By using a piecewise linear function for the inputs, we can ensure that the input signal switches long before the clock transition in order to avoid a setup violation. As it is right now, our script only works for positive-edge triggered flip-flops and should be expanded to handle negative-edge triggered flops.

### *B. Setup Time*

The minimum setup time of a synchronous circuit is defined as the time required for the input signal to be held steady before the clock transition in order to ensure a stable output with an acceptable delay. We define an acceptable delay as a delay that is no worse than 10% of the optimal delay found in the previous section. Our Python script finds the minimum setup time by using a bi-directional search; it runs two simultaneous searches varying the time that the input switches on both sides of the clock transition. Checking the delay of the flip-flop when the input signal transitions from low to high after the clock event may seem trivial because one would not expect to see a change in the output signal. But, there are two reasons that we want to check both sides of the clock. The first is that it is possible to have a flip-flop with a negative setup time. The second reason is that we need to hone in, from both sides, on the input transition time where the delay is forced out of the acceptable delay range. This means that the right side search will move to explore the space where the input transition forces the flip-flop into a meta-stable state and eventually converge to the acceptable delay point.

Our bi-directional search operates as follows:

1) Two searches, L and R, are initiated by setting the input transition times to values both before (to the left of) and after (to the right of) the clock transition.
2) Find the middle point, M, of L and R and run Hspice simulation to find the delay.
   a) If the delay of M is less than the acceptable delay, then L moves to M and repeat step #2.
   b) If the delay of M does not exist or is greater than the acceptable delay, then R moves to M and repeat step #2.
3) When the difference between the input rise times of L and R is less than 1ps, we have found the point where the input transition forces the delay to become 10% worse than the optimal delay.
4) The minimum setup time is the difference between clock transition and the input transition found in step #3.

Our method of finding the minimum setup is accurate to within one picosecond. The accuracy can be adjusted; but an increase in accuracy results in more iterations of the bi-directional search and an increase in runtime. This increase in runtime can become very significant as the supply voltage decreases into the subthreshold range. The increase in delay of the flip-flop at lower voltages enlarges the time window that the Hspice transient analysis is performed on.

## III. Power Analysis

The power analysis of the flip-flop is executed using the Hspice ".measure avg power" statement. This power measurement includes the power dissipation seen by the switching event of the flop, the clock signal, and the data signal. For this measurement, we change the clock signal from a piecewise linear function to a pulse. The average power is measured over two full clock periods so that the power from storing both a 0 and a 1 is considered. We adjust the frequency of the clock pulse based on the calculated Clk-Q delay and minimum setup time to ensure that the entire switching event of the flip-flop is captured. Recall that as the supply voltage decreases, the propagation delay increases resulting in a lower frequency clock signal. We can estimate the clock frequency using

$$T \geq t_{clk-q} + t_{logic} + t_{setup}. \quad (1)$$

The minimum clock period T must be greater than or equal to the sum of the Clk-Q delay ($t_{clk-q}$), the worst case logic delay ($t_{logic}$), and the setup time ($t_{setup}$). In our case, $t_{logic}$

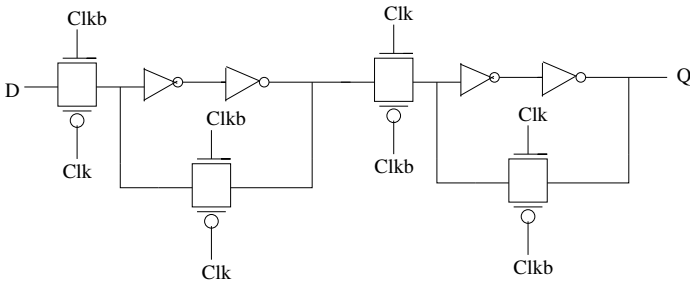


Fig. 2. D-type Master-Slave Schematic

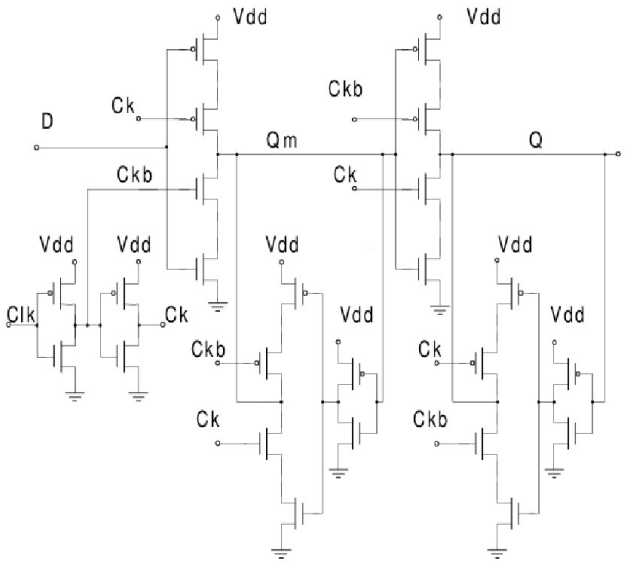


Fig. 3. mC$^2$MOS Schematic [4]

is negligible because we are only focused on analyzing the flip-flop.

## IV. Experimental Results

Simulations are performed using a 180nm TSMC technology. The threshold voltages for the NMOS and PMOS devices are $V_{thn}$ =0.362V and $V_{thp}$ =-0.406V. We simulate the following flip-flop designs in 100mV steps from 1V to 200mV:

- D-type Master-Slave transmission gates (Figure 2)
- mC$^2$MOS Master-Slave (Figure 3)
- PowerPC 603 Master-Slave (Figure 4)

A previous work [3] found the PowerPC 603 Master-Slave to be the most energy-efficient by the PDP metric at subthreshold voltages. Using super-threshold voltages, the mC$^2$MOS Master-Slave was slightly less energy-efficient than the PowerPC design, but it has not been analyzed in the subthreshold region.

It is important to note that the input signals are buffered using inverters. Without a buffer, the ideal voltage source has zero internal resistance and can supply infinite current. Buffering the input signals provides a more realistic signal with a skew that is adjusted based on the supply voltage value.

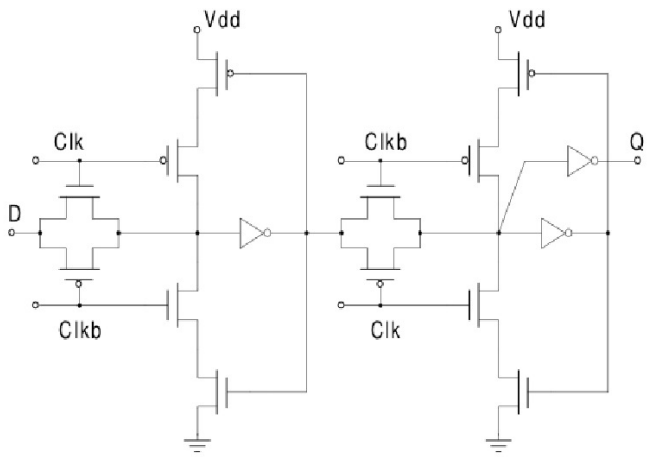


Fig. 4. PowerPC 603 Master-Slave Schematic [4]

The Clk-Q delay, minimum setup time, average power, and power-delay product for each flip-flop design at the different voltage levels are displayed in Tables 1-3. In the tables, "NA" denotes that the simulated design did not operate reliably at the specified voltage. We classify the energy efficiency as the power delay product (PDP). The power delay product is defined as the average energy consumed by the flip-flop per switching event according to

$$PDP = P_{avg}(t_{clk-q} + t_{setup}) \tag{2}$$

where

$$P_{avg} = \frac{1}{T}\int_0^T p(t)\,\mathrm{d}t \tag{3}$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,\mathrm{d}t. \tag{4}$$

There is an interesting trade-off between the delay, setup time, and average power consumption of the three flip-flop designs. At voltages over 800mV, our results agree with prior works [4]. The PowerPC flip-flop has better Clk-Q delay, smaller minimum setup times, and lower power dissipation making it the most energy-efficient. In fact, at all supply voltages the PowerPC flip-flop is the most efficient in terms of the power delay product; agreeing with the findings of several prior works [2], [3]. Figures 5, 6, 7, 8 illustrate the Clk-Q delay, minimum setup times, average power consumption, and power delay products of each design, respectively.

As the supply voltage decreases below 800mV we do see some interesting behavior amongst the flip-flop designs. The mC$^2$MOS actually has better Clk-Q delay than the PowerPC flip-flop at all voltages below 800mV, but it has significantly worse setup times. The drastic difference in setup times outweighs the increased Clk-Q performance seen by the mC$^2$MOS design and the PowerPC maintains its efficiency

| D-type Master-Slave | | | | |
|---|---|---|---|---|
| Voltage | Clk-Q (ns) | Setup (ns) | Avg Power ($\mu$W) | PDP (fJ) |
| 1V | 0.35097 | 0.19389 | 13.692 | 7.4602 |
| 900mV | 0.45142 | 0.27195 | 11.412 | 8.2551 |
| 800mV | 0.63918 | 0.41831 | 4.8145 | 5.0913 |
| 700mV | 1.0934 | 0.74363 | 1.5198 | 2.7919 |
| 600mV | 2.8500 | 1.6431 | 0.55442 | 2.4912 |
| 500mV | 14.483 | 5.0461 | 0.092682 | 1.8100 |
| 400mV | 114.56 | 27.274 | 0.0077936 | 1.1054 |
| 300mV | 1020.8 | 259.52 | 0.00052082 | 0.66682 |
| 250mV | 2977.5 | 892.33 | 0.00011018 | 0.42638 |
| 200mV | 8162.0 | 3269.0 | 0.000034509 | 0.39447 |

TABLE I
TIMING AND POWER DATA FOR D-TYPE MASTER-SLAVE FLIP-FLOP. THIS DESIGN IS THE LEAST EFFICIENT IN THE SUPER-THRESHOLD REGION BUT IS MORE EFFICIENT THAN THE MC$^2$MOS IN THE SUBTHRESHOLD REGION BY THE PDP.

| mC$^2$MOS | | | | |
|---|---|---|---|---|
| Voltage | Clk-Q (ns) | Setup (ns) | Avg Power ($\mu$W) | PDP (fJ) |
| 1V | 0.31677 | 0.16492 | 13.656 | 6.5780 |
| 900mV | 0.41201 | 0.22864 | 10.752 | 6.8883 |
| 800mV | 0.58194 | 0.35713 | 4.7844 | 4.4930 |
| 700mV | 0.9549 | 0.69138 | 1.4715 | 2.4225 |
| 600mV | 2.1878 | 1.9998 | 0.54262 | 2.2723 |
| 500mV | 9.4141 | 10.739 | 0.09117 | 1.8374 |
| 400mV | 70.816 | 82.805 | 0.0075325 | 1.1572 |
| 300mV | 623.78 | 790.84 | 0.00051485 | 0.72832 |
| 250mV | 1834.9 | 2452.4 | 0.00011542 | 0.49484 |
| 200mV | NA | NA | NA | NA |

TABLE II
TIMING AND POWER DATA FOR THE MC$^2$MOS FLIP-FLOP. THE MC$^2$MOS HAS THE LOWEST CLK-Q DELAY AT VOLTAGES BELOW 800MV BUT HAS SIGNIFICANTLY WORSE SETUP TIMES IN COMPARISON.

edge by the PDP metric. We also observe that the mC$^2$MOS flip-flop consumes less power than the D-type master slave in the super-threshold region from 500mV to 800mV. But, at subthreshold voltages, the D-type master slave actually consumes less power than the mC$^2$MOS. Coupled with smaller setup times, the D-type master slave is more efficient than the mC$^2$MOS while operating in the subthreshold voltage region. This illustrates the fact that a flip-flop that is efficient at super-threshold voltages may not be a good design choice at subthreshold voltages. Lastly, we observe that D-type master slave is the most robust design and can operate reliably at lower voltages.

There are approaches to subthreshold circuit design that help to increase efficiency and reliability. Minimum size devices can be used to minimize the energy consumption per operation, but this approach may have an overhead of increased delay [5]. [5] has also shown that devices can be strategically sized to lower the minimum operating voltage. Sizing the PMOS and NMOS devices at a 12:1 ratio allows for reliable operation at lower subthreshold voltages, but this increases the total energy consumed at a given voltage. Following this sizing ratio will ensure a robust and reliable design.

| PowerPC 603 Master-Slave | | | | |
|---|---|---|---|---|
| Voltage | Clk-Q (ns) | Setup (ns) | Avg Power ($\mu$W) | PDP (fJ) |
| 1V | 0.30711 | 0.15411 | 11.937 | 5.5056 |
| 900mV | 0.39681 | 0.21330 | 9.9368 | 6.0625 |
| 800mV | 0.56682 | 0.32136 | 4.1893 | 3.7209 |
| 700mV | 0.98991 | 0.54179 | 1.3712 | 2.1003 |
| 600mV | 2.6998 | 1.0637 | 0.49972 | 1.8807 |
| 500mV | 14.322 | 3.3558 | 0.084548 | 1.4946 |
| 400mV | 114.99 | 19.647 | 0.0071601 | 0.96401 |
| 300mV | 983.55 | 152.59 | 0.00047737 | 0.54236 |
| 250mV | 2771.3 | 472.11 | 0.00010492 | 0.34030 |
| 200mV | NA | NA | NA | NA |

TABLE III
TIMING AND POWER DATA FOR THE POWERPC 603 MASTER-SLAVE FLIP-FLOP. IT IS THE MOST EFFICIENT DESIGN AT ALL VOLTAGES BY THE PDP.

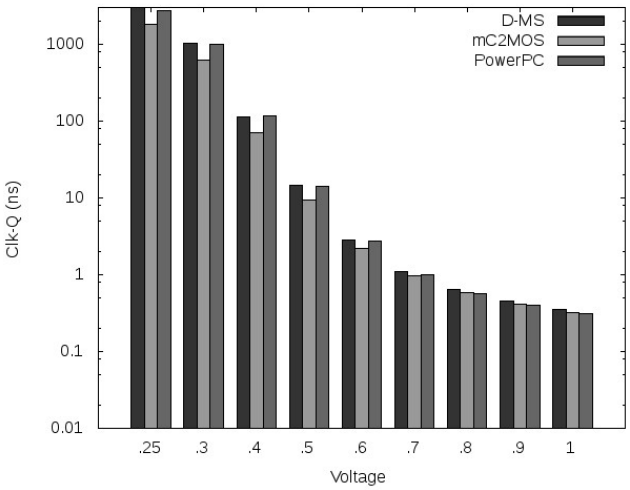


Fig. 5. Comparison of the Clk-Q delay of the different flip-flops at various supply voltages.

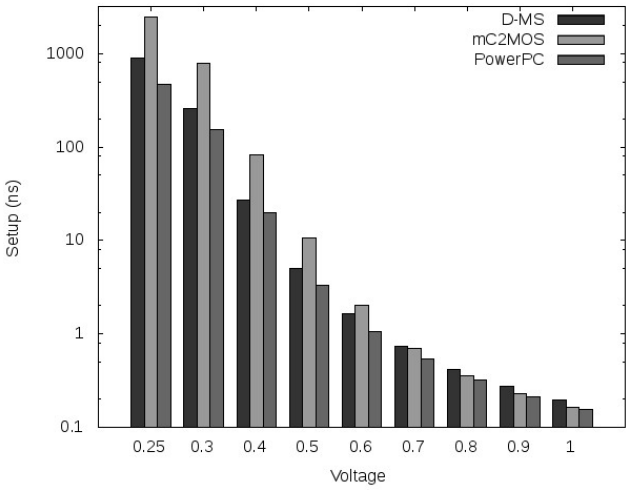


Fig. 6. Comparison of the setup times of the different flip-flops at various supply voltages.

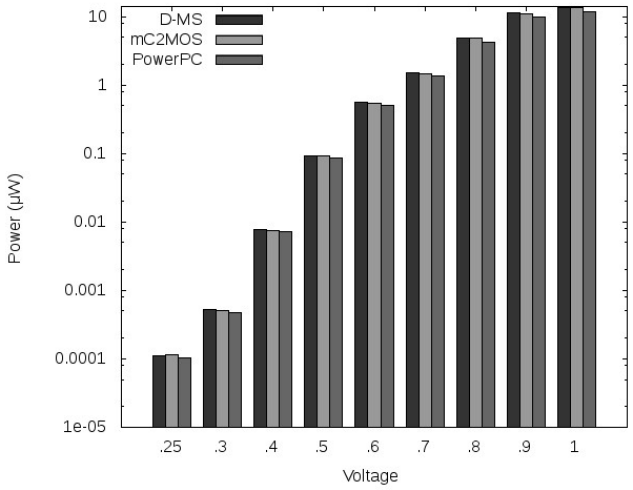


Fig. 7. Comparison of the average power of the different flip-flops at various supply voltages.

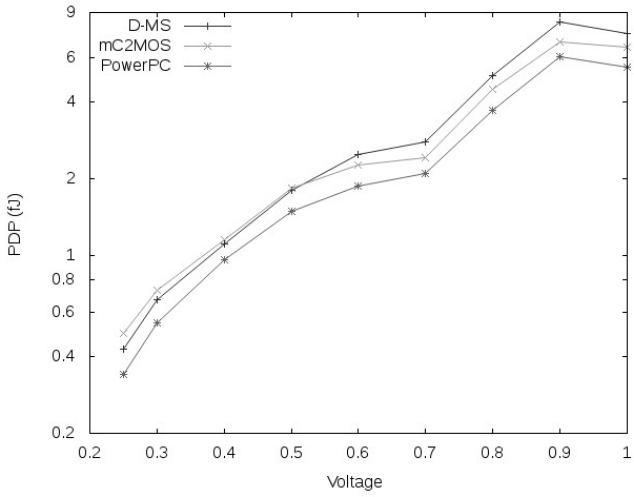


Fig. 8. Comparison of the PDP product of the different flip-flops at various supply voltages.

## V. Conclusion

This paper has introduced a methodology for characterizing the energy-efficiency of flip-flop designs at both super- and sub-threshold supply voltages. We use this methodology to analyze three master-slave flip-flop designs from 1V to 200mV. We provide their Clk-Q delays, minimum setup times, average power consumption, and characterize their energy-efficiency in term of the power delay product. Of the flip-flops analyzed, we find that the PowerPC 603 master-slave design is the most efficient in both the super- and sub-threshold voltage region. We also find that efficient super-threshold flip-flop operation does not guarantee efficient sub-threshold operation, as illustrated by the D-type master-slave in comparison to the mC$^2$MOS flip-flop.

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