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# A Methodology for Characterizing Cell Testability

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# A Methodology for Characterizing Cell Testability

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## ABSTRACT

Integrated circuits (ICs) are continually increasing in complexity. As IC complexity increases, the cost of testing the IC also increases. As a result, IC designers are expending greater amounts of effort on designing the ICs to be more easily tested. Most of the work done in measuring the testability of ICs and modifying the ICs to improve testability has been focused at the schematic level. This dissertation defines a metric for measuring the testability of cells used in ICs at the physical design level. This testability metric takes into account the three major influences on testability: the physical design, the circuit schematic, and the methods used to test the circuit. IC designers can use this testability metric as a guide for modifying the physical design of logic cells to increase their testability. This dissertation shows that, for standard cell designs, designing the cells to be more testable will have a larger impact on the testability of the circuit than designing other parts of the circuit. Thus, the testability metric described here concentrates on the cells used in standard cell designs. This dissertation describes an implementation of the testability metric. This dissertation applies the metric to two cells from a standard cell library to demonstrate how cell testability can be used to guide the modification of the cell's physical design to improve its testability.

**Keywords:** Testability, Carafe, Design for Test, Inductive Fault Analysis

# Chapter 1

# Introduction

Integrated circuits (ICs) are tested after they are manufactured to ensure that ICs sent to the customer are free from manufacturing defects that may affect their operation. As IC complexity increases, the cost of testing the IC increases due to the higher cost of test equipment and longer periods of time required to fully test the IC. Unfortunately, IC designers address testing after many other aspects of IC design have been completed, thus making completely testing the IC difficult or impossible. This dissertation presents a methodology that estimates the effective testability of the logic cells in a circuit. IC designers can use this methodology to modify the logic cells to increase their effective testability.

## 1.1 Designing Testable Cells

The goal of IC testing is to ensure that no defective ICs are delivered to customers. The success of testing is the fraction of fault-free ICs among those that pass all of the tests. This measure is known as the quality level (QL) and is often reported by the complementary term, defect level (DL), where $QL = 1 - DL$. DLs are typically much less than 200 defects per million(DPM) [27][40]. Previous work has shown that achieving high quality levels requires being able to detect a very high percentage of the defects that may occur during the manufacture of the IC [10][26][27][41]. Also, the present methods of generating tests for ICs do not detect many of the defects that may occur in current CMOS processes [12][16][36][39]. For example, the short depicted in Figure 1 behaves like a logic AND gate in one family of standard cells. Since the two shorted lines are inputs to a NAND gate, the effect of the short cannot be detected by observing the logic values at the output of the NAND gate. This may lead some to believe that the short is innocuous since it does not affect the logic behavior of the circuit. However, the short can cause an increase in power supply current, which may

cause the circuit to be unreliable or prone to failure. Therefore, the detection of many apparently innocuous faults is desirable.

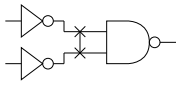

**Figure 1** Example wired-AND short that cannot be detected as a logic fault.

The cell-based design style is one of the most popular methods used to design circuits [32]. In this design style, the individual logic cells or gates are designed once and stored in a library. When a circuit designer requires a cell that implements a given logic function, the designer retrieves the cell from the library and instantiates the cell into the circuit. This design style also facilitates automated circuit design by allowing design tools to concentrate on placing cells and routing the interconnection wires as efficiently as possible. IC designers primarily address cell performance and area during the creation of the cells, whereas designers seldom address the testability of the cells during cell creation.

This dissertation contains a description of an investigation into designing cells to be easily testable. Although creating a circuit with testable cells does not guarantee that the circuit is testable, the testability of the cells limits, or places an upper bound on, the testability of the circuit. This dissertation links the testability of cells to the testability of the circuit and introduces a cell testability measure. This cell testability measure includes the effects of the test environment and the circuits in which the cells are used. Cell designers can use this methodology to identify which faults may be difficult to detect in a cell. This information can guide cell designers to create cells that not only have high performance and little area, but also have a high level of testability.

## 1.2 Dissertation Organization

Chapter 2 defines the terms used throughout this dissertation and provides a review of previous research in design for testability (DFT).

Chapter 3 develops the relationships between quality level and useful testability metrics. Chapter 3 also presents and discusses the major influences on testability. This chapter finishes by outlining a methodology that can be used to estimate the testability of IC components and thus, the expected quality levels for the IC.

Chapter 4 investigates the potential benefits that can be gained from designing cells to be testable. This chapter examines cell-based circuits to determine which parts of the circuits are more likely to contain defects and cause faulty behavior. Fault simulation of the faults that may occur in the circuits shows which faults are more difficult to detect. The difficult to detect faults indicate which parts of the circuits will benefit the most from physical design for testability and also how much benefit can be realized. This chapter also introduces the types of defects and faults that will be examined in this dissertation, as well as the tools and techniques used to analyze the circuits and cells in the presence of these faults.

Chapter 5 presents a methodology for measuring a logic cell's effective testability. This methodology determines the testability of each fault within a cell with respect to the test environment and the circuit topology. The methodology correlates the faults that may occur in the cell as a result of manufacturing defects with characterizations of the test environment and the circuit topology to compute the effective testability of the cell. This information can guide cell designers to create cells that are more testable for the given test environment and class of circuits.

Chapter 6 contains an example application of the methodology described in Chapter 5. Using the characterizations produced by the methodology, this chapter analyzes the testability of a few cells. This chapter then presents physical modifications made to the cells to increase their testability.

Chapter 7 summarizes the contributions of this dissertation. This chapter also proposes areas of future research.

# Chapter 2

# Background

The term testability means many things to different people. There currently is no single accepted definition of testability. This chapter reviews some of the work that has been done to define testability and work that has been done to quantify testability. Most of these also provide examples of how the circuit can be modified to increase the circuit's testability as they have defined it. The first section of this chapter defines some of the terms that are used throughout this dissertation. The second section briefly describes work done previously in defining testability and developing DFT techniques.

## 2.1 Definitions

The first set of definitions describes the levels of abstraction of IC failures. The next set of definitions describes terms relating to the measurement of testability and terms that distinguish a circuit and its components. These terms are also defined in the Glossary in Appendix A.

There are several levels of abstraction that describe the effects of failures in ICs as a result of manufacturing problems [2]. The abstraction levels start at the physical failure mechanisms and progress through different interpretations of the behavior of the fabrication anomaly. The diagram in Figure 2 shows the different abstraction levels from the lowest, the failure mechanism, to the highest, the high-level fault. The diagram also shows relationships between the levels of abstraction. In some cases, more than one item at one level of abstraction may cause the same effect at the next higher level of abstraction. A simple example of this is a short between two wires on an IC. There are many possible, independent physical defects that can cause extra