An Unexpected Factor in Testing for CMOS Opens: The Die Surface

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ABSTRACT

In this paper, we for the first time present experimental evidence that the die surface can act as an RC interconnect, becoming an important factor in determining the voltage of a floating wire created by a CMOS open. We present a circuit model for this effect verified with HSPICE simulations. A detailed analysis of potential mechanisms behind this phenomenon is provided. We also present our measurement results for the trapped charge deposited on floating gates during fabrication.

1. Introduction

As part of our research on testing for CMOS opens, we became interested in the amount of electrical charge trapped on the floating gates of CMOS transistors that are disconnected from their drivers due to breaks in the interconnect. This charge is important, because it is one of the factors that determine the voltage on a floating gate [10] [2] [7] [4] [12], thus determining the behavior of the faulty cell this floating-gate transistor is in. Johnson [5] designed and performed trapped charge measurements on test structures that consist of floating-gate p-channel and n-channel transistors with varying lengths of poly extensions. These measurements showed that there was always a positive charge on the floating poly, and the voltage created by this charge ranged from 0.1V to 2.3V.

We built our own floating-gate test structures to measure the effects of different lengths and different layers of floating metal lines connected to transistor gates. In a standard cell design, most of the area is taken by the metal interconnect. Therefore, the likelihood of a break in the interconnect is greater than the one inside a cell. Moreover, not all breaks inside a cell create floating-gate transistors. They may create, for instance, network breaks [6]. In addition to observing the effects of different metal layers and metal lengths on the amount of trapped charge, we also wanted to try erasing this charge via ultra-violet light as done for EPROMs.

Our experiments took a very unexpected turn when we noticed that the floating-gate voltages in our hermetically sealed packages were behaving differently from the ones in other packages with their dies exposed to air. The floating-gate voltages in the sealed packages displayed a swing of at least 0.5V with a short rise time and a long fall time, while the other packages did not. We had to conduct several experiments to identify what was really going on, and possible mechanisms behind it. All of our experimental data, as we explain starting from Section 3, point to the conclusion that the die surfaces in our hermetically sealed packages are conducting sufficient electrical charge forming an RC path from all other signals in the chip to the metal wires connected to the floating gates. The time constant of this path is varying from a couple of seconds to a couple of minutes. Because, a part typically spends from a couple of seconds to a couple of minutes on a tester, the die surface becomes a determining factor on the behavior of a floating gate during the period the part is tested. The capacitance of a wire in a VLSI chip today is typically between 10^{-15}F to 10^{-12}F. In order to obtain a time constant of 1 second, a resistance of $10^{12}\Omega$ to $10^{15}\Omega$ is needed, which is a perfect insulator for normal operation of the chip, but conductive enough to affect the voltage of a floating-gate.

Until now, the voltage of a wire connected to one or more floating gate transistors due to a break in the interconnect is thought to be determined by only two factors: *i)* the coupling capacitances to neighboring wires and to other terminals of the floating gate transistors, and *ii)* the amount of the trapped charge deposited on the floating gates during fabrication. In this paper, we present several experimental evidence that the die surface conduction forms the third factor in determining the voltage of a floating wire. We first present in Section 3 the phenomenon we have observed that led us to the die surface, and then in Section 4 we analyze several mechanisms that might be responsible for die surface conduction, and we present evidence for or against these mechanisms including HSPICE simulation results matching the floating-wire behaviors we have observed.

In the following section we will first describe our test chip and the measurement technique we used. We will then present how the die surface is involved in determining the floating-gate voltages, and finally we will present our trapped charge measurement results, since they became a secondary issue compared to the die surface conduction.

2. The Test Chip and the Measurement Technique

Our test chip was fabricated using the HP 0.8μ CMOS n-well technology through MOSIS. Twelve of our packages are hermetically sealed with metal lids, and thirteen of them have their die cavities covered by taped plastic lids so that these lids can be easily removed by peeling off the tape to be able to expose the die to ultra-violet light. All of our packages are ceramic.

In our test chip, we have three n-channel transistors with 125μ, 250μ, and 500μ long metal-2 wires attached to their gates. These wires are not driven by any other device, and they are all 1.5μ wide. For each such floating-gate wire g, two metal-2 wires are running on both sides of g with a separation distance of 1.5μ from g. Connected to these two metal-2 wires, a metal-1 wire is running just below g, forming an electrical node pg (pseudo gate). The voltage on floating gate g can be controlled by controlling the voltage on pg because of the capacitance between pg and g. We use an identical n-channel transistor in order to measure the voltage on g.

Figure 2.1 shows our measurement circuitry. The dotted rectangle represents the chip boundary. Everything outside the dotted rectangle is off-chip. The n-channel transistor on the left in Figure 2.1 represents the floating gate transistor, and the one on the right represents the identical size reference transistor. All the transistors on our test chip are 0.8μ long and 5μ wide. The basic idea to measure the floating-gate voltage is to apply the same drain-source voltage to both transistors, and to have the same drain current flowing through both transistors. In this state, the measured gate voltage on the reference transistor will be the same as the gate voltage on the floating-gate transistor. This method is also used by Johnson [5], but our measurement technique shown in Figure 2.1 keeps the drain-source voltage fixed at 0.2V, thus eliminating the hot electron effect that might otherwise alter the amount of the trapped charge, as we explain in Section A.2. The op-amps in Figure 2.1 also make sure that the same current is flowing through both transistors.

We refer to the voltage on the floating gate when all the chip pins are grounded as the **trapped charge voltage**. The basic idea to measure the trapped charge voltage is to measure at least two points on the $V_g - V_{pg}$ plane, and extrapolate to $V_{pg} = 0$ assuming a linear relationship between V_g and V_{pg}. The actual relationship is

$$V_g = K1 * V_{pg} + K2 * V_{ds} + V_{tc} \quad \text{where} \tag{2.1}$$

$$K1 = \frac{C_{pg-fw}}{C_{pg-fw} + C_{fw} + C_{gate}}, \quad K2 = \frac{C_{gd}}{C_{pg-fw} + C_{fw} + C_{gate}}$$

C_{pg-fw} and C_{fw} are the capacitances from pg to the floating wire in Figure 2.1 and from the floating wire to the substrate, respectively. The gate capacitance is the sum of the gate-to-drain, gate-to-source, and gate-to-bulk capacitances, that is, $C_{gate} = C_{gd} + C_{gs} + C_{gb}$. V_{tc} is the trapped charge voltage, and V_{ds} is the drain-source voltage, which is kept fixed at 0.2V. The Appendix shows that $K2 * 0.2$ is less than 15mV. The value of $K1$ changes slightly as the transistor enters the linear region from the cut-off region, introducing a slight extrapolation error, as explained in the Appendix.

In our test chip, we also have three n-channel floating-gate transistors with poly extensions of 42μ, 21μ, and no extension. No metal is attached to these floating gates, and the width of the poly is 1μ. Over both the 42μ and 21μ poly extensions, we have a metal-1 rectangle that is 12μ wide, creating the pg node shown in Figure 2.1.

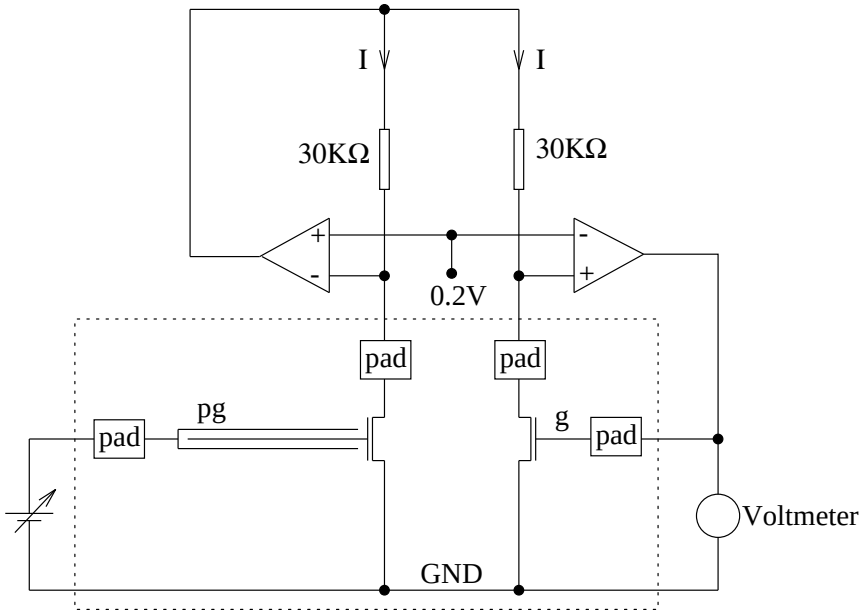

Figure 2.1: Circuitry to measure the floating gate voltage controlled by *pg*

We have three p-channel floating-gate transistors with metal-1, metal-2, and metal-3 wires attached to their gates. Each such wire is 250μ long. Both the metal-1 and metal-2 wires are 1.5μ wide, but the metal-3 wire is 3μ wide, which is the minimum width for metal-3 according to MOSIS rules. These metal wires are not surrounded by any other wire, that is, we can control the floating-gate voltage only by controlling the source-drain voltage. This is also the technique used by Johnson [5]. Figure 2.2 shows our measurement circuitry for this technique. A similar circuit is also used by Pricket et al. [8]. The main reason we did not create a *pg* node around the floating wires of these three p-channel transistors is that estimating the capacitance of a floating wire to *pg* and to substrate becomes very hard based on the capacitance parameters given by MOSIS, because these parameters do not include wire-to-wire capacitance on the same layer, and the given capacitance parameters assume a wire-on-a-plane structure. So, it is very easy to estimate the substrate capacitance of a floating wire not surrounded by any other wire. We wanted to know the total capacitance of the floating wire in order to be able to compute the amount of the trapped charge from our V_{tc} measurements.

The main difference in the technique used in Figure 2.2 compared to Figure 2.1 is that the source-drain voltage is not constant, and it is used to control the floating-gate voltage. Note that the drain-source voltages for the floating and the reference transistors are kept the same by the op-amp. All of our op-amps have their outputs connected to a 10μF capacitor to prevent oscillation, which is not shown in Figures 2.1 and 2.2.

In Figure 2.2, the basic idea to measure the trapped charge voltage is to measure at least two points on the $V_g - V_{source}$ plane, and extrapolate to $V_{source} = 0$. The assumption is

$$V_g = K3 * V_{source} + V_{tc} \quad \text{where} \quad K3 = \frac{C_{gs} + C_{gb}}{C_{fw} + C_{gate}} \tag{2.2}$$

The bulk (n-well) of the transistor is tied to the source terminal in our p-channel transistors. The Appendix shows the extrapolation errors for this case.

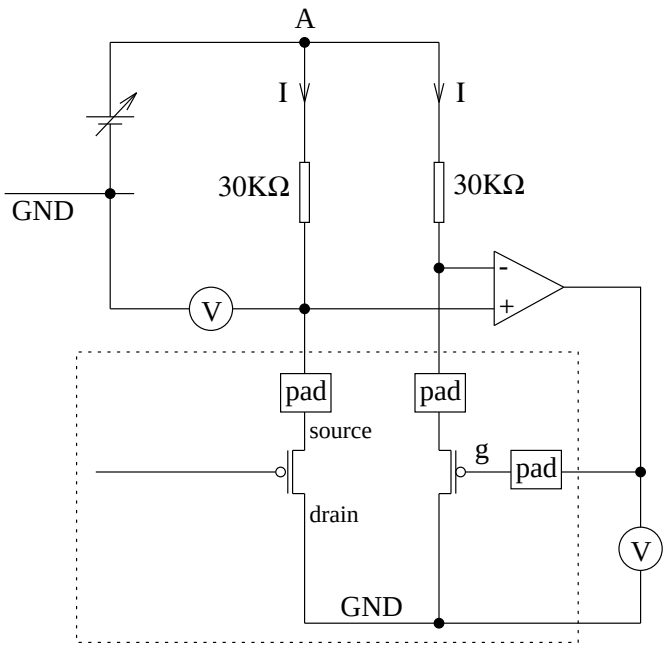

Figure 2.2: Circuitry to measure the floating gate voltage controlled by source

We also have three other p-channel floating-gate transistors with poly extensions the same as the three n-channel transistors described earlier. The only difference is that the metal-1 over the poly extension is grounded, and the measurement circuitry in Figure 2.2 is used. Table 2.1 summarizes the twelve floating-gate (**FG**) transistors we used. The measurement technique for transistor 6 is similar to the one used for p-channel transistors, because the setup for transistor 6 does not have a *pg* node.

n-channel transistors: FG voltage controlled by *pg* voltage		p-channel transistors: FG voltage controlled by *source* voltage	
trans. #	FG extension	trans. #	FG extension
1	500μ metal-2	7	250μ metal-1
2	250μ metal-2	8	250μ metal-2
3	125μ metal-2	9	250μ metal-3
4	42μ poly	10	42μ poly
5	21μ poly	11	21μ poly
6	no extension	12	no extension

Table 2.1: Summary of the twelve floating-gate (FG)transistors in our test chip

3. The (Mysterious) Effect of the Vdd-Ring

On our chip, we have a 50μ wide metal-3 wire, called Vdd-ring, that goes all around the die periphery through the pad cells to supply the Vdd voltage to electrostatic discharge protection circuits inside the pad cells. What looked very mysterious was that the FG voltage of any transistor with a metal wire connected to it was quite unstable when we applied 5V to the Vdd-ring. This applies to the transistors 1–3 and 7–9 in Table 2.1. More specifically, switching the Vdd-ring voltage from 0V to 5V caused the FG voltages of transistors 1 through 3 go from around 1.0V to around 1.5V within 5 seconds to a couple of minutes depending on the package. The FG voltage would then turn back, and go down to its previous value before 5V was applied to the Vdd-ring, which took about 3 minutes to about an hour. Both the rates of increase and decrease in FG voltage resembled an RC charge-up or an RC discharge. We observed the same type of behavior for transistors 7 through 9. The FG voltages of transistors 7, 8, and 9 in one package increased 0.66V, 0.92V, and 1.43V, respectively, using the setup shown in Figure 2.2. In this particular experiment, we kept the voltage of node A constant, but as the gate voltage increased, the drain-source voltage also increased, unlike the setup in Figure 2.1, where the drain-source voltage is always 0.2V. The FG voltages reached their peaks within 3-5 seconds again displaying an RC charge-up, and came back to their previous values within 2-3 minutes at the rate of an RC discharge. Transistors 7–9 in other hermetically sealed packages showed the same behavior but only taking a longer time, up to 45 minutes, to complete the cycle of RC charge-up and RC discharge.

The gate voltages of all other FG transistors showed only a couple of millivolts of reaction to the Vdd-ring. Note that all of these other FG transistors have only poly extensions to their gates, if any, and all the poly extensions are covered with metal-1.

A very important observation is that switching the Vdd-ring voltage from 0V to 5V had no effect on the FG voltage of any transistor in the taped-lid packages, even though the dies in all our packages are identical. That is, we observed the effect of Vdd-ring only in the hermetically sealed packages. This shows that there is no direct capacitive coupling between the Vdd-ring and the FG wires. Because, if there was, we would observe the same behavior in the taped-lid packages also. Besides, the distance between the Vdd-ring and the long side of any other FG wire is between 100μ to 600μ, which is too large a distance to have any coupling capacitance.

We carefully removed the metal lid of an hermetically sealed package to see whether the Vdd-ring effect would disappear. To our expectation, the Vdd-ring effect has indeed completely disappeared. We very carefully drilled a very tiny hole, less than $1mm$ in diameter, through the metal lid of another hermetically sealed package. About 5 minutes after drilling the hole, switching Vdd-ring from 0V to 5V caused a diminished effect on the FG voltage of transistor 9. The following day, the Vdd-ring effect has completely disappeared. This was an evidence that air entering the die cavity has something to do with this phenomenon.

We learned from MOSIS [3] that in the case of hermetic sealing the packages are placed in a closed oven, where the chips are cleared of moisture at a temperature of 150°C by passing dry nitrogen through the oven. The packages are then sealed by covering the die cavity with a metal lid soldered using the gold eutectic solder ring around the lid. So, the die surface in touch with air versus the die surface cleared of moisture and in touch with dry nitrogen is making the difference.

We speculate that the die surface is somehow involved in charge transport. We came up with the circuit shown in Figure 3.1 modeling the Vdd-ring effect we observed. The cross sections of the floating wire and the Vdd-ring are shown. The floating wire is connected to a transistor gate, which is not shown in the figure. $C_{fw-subs}$ and $C_{fw-surf}$ denote the capacitances from the floating wire to the

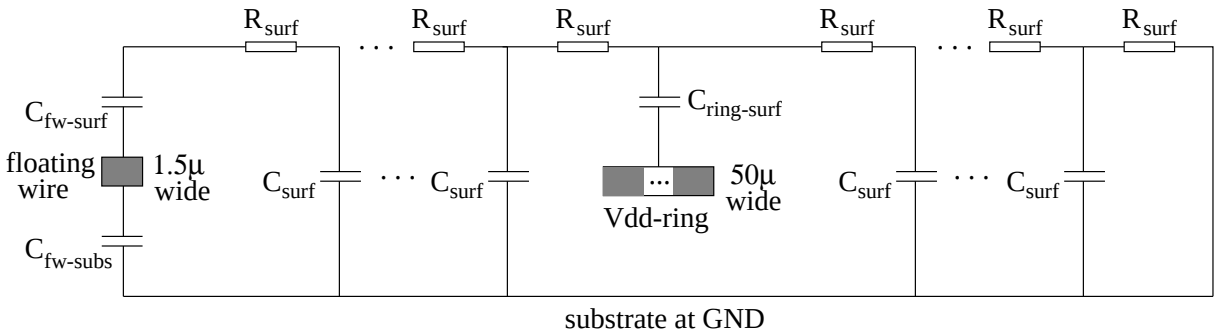

Figure 3.1: The circuit modeling the effect of the Vdd-ring

substrate and to the die surface, respectively. The RC path $\{C_{ring-surf}, R_{surf}, ..., R_{surf}, C_{fw-surf}\}$ from Vdd-ring to the floating wire in Figure 3.1 models the RC charge-up we observed in our experiments. As we mentioned earlier, the FG voltages of transistors 7, 8, and 9 in one package increased 0.66V, 0.92V, and 1.43V, respectively, showing that metal-3 is affected the most by the Vdd-ring, followed by metal-2 and metal-1. So, as the floating wire gets closer to the die surface, it becomes more influenced by the voltage change on the Vdd-ring, which supports our die surface conduction speculation. It does not surprise us that Johnson [5] has not reported any such phenomenon, because all of the poly extensions in his FG transistors were covered by metal lines connected to transistor drains or sources, which shielded the poly extensions from the die surface. As explained earlier, the poly extensions of our transistors 4, 5, 10, and 11 in Table 2.1 are also covered with metal-1, and these transistors are not affected by the voltage change on the Vdd-ring, which is further evidence of die surface conduction.

The RC path $\{C_{ring-surf}, R_{surf}, ..., R_{surf},$ substrate$\}$ in Figure 3.1 models the observed RC discharge. This path implies that the surface must have a path to the substrate, which is indeed the case. The passivation layer touches the bare silicon around the periphery of the die. This way, cutting the dies from the wafer is done by cutting through the bare silicon. Otherwise, cutting through the oxide might crack the oxide layers. The die surface is modeled as an RC interconnect, with extremely high resistance values producing RC time constants that are on the order of seconds and minutes. Air is substantially decreasing the resistances in Figure 3.1 due to the humidity, resulting in very small RC time constants to observe the Vdd-ring effect.

Even though we refer to the effect of the die surface conduction as the Vdd-ring effect, because we have first noticed it by switching the voltage on the Vdd-ring wire, all the signal wires in a regular chip will be affecting the floating-wire voltage via die surface conduction. The Vdd-ring wire in Figure 3.1 can be replaced by any signal wire. Because a signal wire is typically a much smaller wire than the Vdd-ring, the $C_{ring-surf}$ capacitance in Figure 3.1 will be much smaller in the case of a signal wire. Because there are thousands or millions of signal wires in a chip, their combined effect will be much stronger than the Vdd-ring.

In the following Section, we go through possible mechanisms for die surface conduction, and show whether they fit our observations. We want to emphasize that the surface conduction we are talking about has extremely high resistance, but when combined with extremely low capacitances of the wires in the chip, the resulting RC time constant becomes on the order of seconds. We will also present our HSPICE simulation results with the circuit in Figure 3.1, that match the behavior we observed in our experiments.

4. Analysis of Possible Mechanisms for the Vdd-ring Effect

4.1 Is It the Passivation Layer?

One candidate for charge transport on the die surface is the passivation layer. In the HP 0.8μ technology our chips were fabricated with, two passivation layers are used. First, a 0.35μ silicon oxynitride film is deposited on top of the metal-3 layer, followed by a 0.60μ silicon nitride film. Rabiller et al. [9] reported that the room temperature resistivity varies smoothly from less than $10^{14}\Omega - cm$ for silicon nitride to more than $10^{16}\Omega - cm$ for silicon dioxide by varying the ratios of oxygen and nitrogen in a silicon oxynitride film deposited using plasma enhanced chemical vapor deposition (PECVD). Therefore, in our chip we expect the nitride passivation layer to be 100 to 1000 times more conductive than the intermetal dielectric, which is silicon dioxide.

The floating wire of transistor 3 in Table 2.1 starts from a point 85μ away from the Vdd-ring, and extends 125μ into the chip as shown in Figure 4.1. It is 300μ away from the closest parallel Vdd-ring wire. As a crude approximation, let us assume that charge needs to travel 100μ from above Vdd-ring to above the floating wire through the 0.6μ thick nitride film. Let's call this path the **nitride path**. The metal-2 floating wire of transistor 3 is surrounded by two other metal-2 lines connected to a metal-1 line below, creating the electrical node pg, as we explained in Section 2. The distance from the floating wire to either of pg's metal-2 lines is 1.5μ. The metal-2 thickness and the separation between metal-2 and metal-1 layers are both around 1μ. Considering that pg has three paths through the oxide to the floating wire, each path being 1.5μ or less long, we can crudely assume that charge needs to travel 1μ from pg to the floating wire through the oxide, which we call the **oxide path**. Assuming a 1 to 1000 ratio for the nitride to oxide resistivities, and recalling that the nitride path is 100 times longer than the oxide path, the resistance of the oxide path must be only 10 times larger than the resistance of the nitride path.

Even though we observed a 0.5V increase in the floating wire voltage due to the Vdd-ring within seconds or a couple of minutes, the FG voltage returned to its previous value, and stayed there

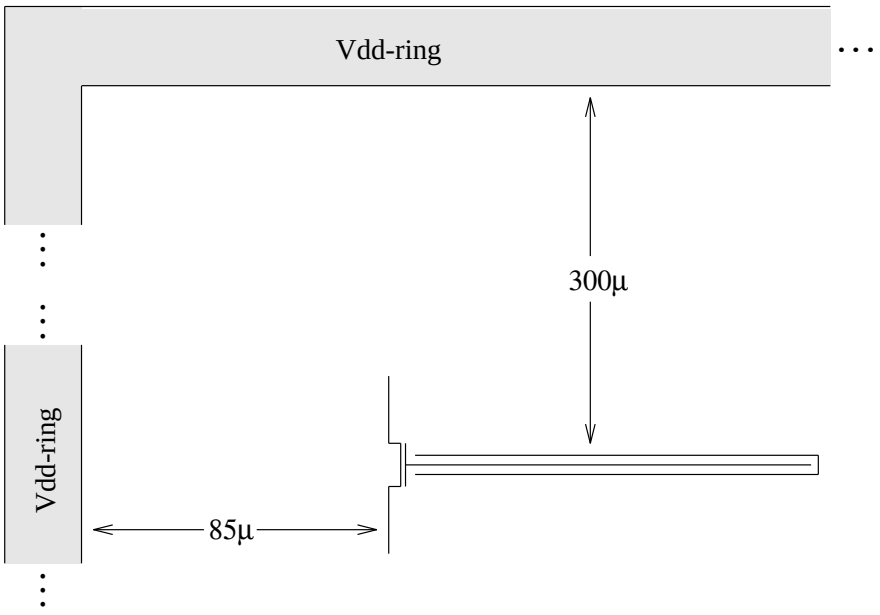

Figure 4.1: The distances between the Vdd-ring and transistor 3

even after an overnight operation with constant *pg* voltage. In other words, in 15 hours we have not observed any RC charge-up through the oxide path, which is at most 10 times more resistive than the nitride path. But, the Vdd-ring effect is observable within seconds, which shows that the nitride cannot be the medium of charge transport for the Vdd-ring effect. Moreover, a substantial portion of the charge traveling through the nitride path will be kept by the surface-to-substrate capacitances shown in Figure 3.1, thus delaying the RC charge-up of the floating wire, which is not the case for the oxide path. Later in this paper, we also show our HSPICE simulation results confirming that the nitride is too resistive to be responsible for the Vdd-ring effect. In addition, it is not clear to us how air would tremendously increase the conductivity of nitride. Recall that the taped-lid packages do not possess the Vdd-ring effect most probably due to the reduction in the surface resistances shown in Figure 3.1 as a result of contact with air.

4.2 Is It the Dry Nitrogen and Air?

Another candidate for the medium of charge transport on or over the die surface is the gas inside the die cavity. This gas is dry nitrogen according to MOSIS in our hermetically sealed packages with metal lids, and ordinary air in packages whose die cavities are covered by taping plastic lids over them. The die cavity is identical in both types of packages, and it is $10mm$ on one side. The distance between the die surface and the plastic or the metal lid is about $1mm$, and the die size is $1.9mm$ on one side. Therefore, applying 5V to the metal lid over the die surface is expected to create a couple of volts of increase in the die surface potential if dry nitrogen is the conduction medium responsible for the Vdd-ring effect. But, we observed only a 1-2mV immediate increase in the FG voltage of transistor 3 after we applied 5V to the metal lid. We observed no further increase at all even after waiting for a couple of minutes, whereas the RC charge-up of the FG voltage of transistor 3 in the same package takes only 30 seconds resulting in a 0.5V increase. Grounding the metal-lid resulted in an immediate 1-2mV decrease in the FG voltage, again followed by no further change at all.

We took the package that we drilled a tiny hole through its metal lid as we described in Section 3, and applied 5V to its lid, also. Again, the behavior was exactly the same as we described above. Therefore, neither air nor dry nitrogen can transport sufficient electrical charge from/to the die surface within minutes to be responsible for the Vdd-ring effect we observed.

There is an additional evidence against the dry nitrogen. After 3 months, both the RC charge-up and discharge of the FG voltages in hermetically sealed packages took about 20 times longer than they used to take initially. For instance, the RC charge-up of transistor 3 took 10 minutes compared to 30 seconds it took 3 months earlier. The RC discharge was also proportionally delayed, but the amplitude remained the same at 0.5V level. If the dry nitrogen is responsible for the charge transport, it is not clear why its resistivity would increase 20 times while it is enclosed under a hermetic seal, and the ambient temperature is about the same. Actually, this observation is evidence against the passivation layer, also.

4.3 A Hygroscopic Film on the Die Surface?

When we mentioned that the Vdd-ring effect disappears when air enters the die cavity by either removing the metal lid or drilling a tiny hole through it, Vance Tyree of MOSIS speculated the existence of a hygroscopic contaminant on the die surface. From the time wafers are fabricated to the time they are cut and packaged at a different location and company they are shipped to, a film of hygroscopic material might be formed on the die surface. When the packages are placed

in an oven at 150°C, and dry nitrogen is passed through the oven, most of the moisture in this hygroscopic material will evaporate, but sufficient amount of moisture may remain to cause the conduction we observed in the hermetically sealed packages. When a hole is drilled through the metal lid, air re-hydrolizes this material on the die surface, substantially decreasing its resistivity, so that any induced charge on the die surface would leak away to the substrate in less than a second. Recall that the die surface terminates at the substrate on the periphery of the die, as explained in Section 3.

In 3 months, more moisture from the hygroscopic film may evaporate into the dry nitrogen inside the hermetic seal at room temperature. This explains why the resistivity of the conducting medium has increased 20 times after 3 months.

In order to estimate the resistance this speculated hygroscopic film needs to exhibit in order to produce the RC behavior we observed, we performed HSPICE simulations using the circuit in Figure 3.1. We attempted to duplicate our RC charge-up and discharge observations for transistor 8 in a typical hermetically sealed package, where the FG voltage in Figure 2.2 increases 0.9V in less than a minute, and comes back to its initial value in less than an hour. In our HSPICE runs, the floating wire in Figure 3.1 is connected to a floating gate pMOS transistor as shown in Figure 2.2, the source and the bulk of the transistor are connected to a 30KΩ resistor, and the drain is grounded.

The floating wire is a metal-2 line 250μ long and 1.5μ wide. From the capacitance parameters provided by MOSIS for run *n4cp* of the HP 0.8μ process, we computed $C_{fw-subs}$ to be 23fF. Because metal-2 might be slightly closer to the die surface than it is to the substrate in this 3-metal process, and the dielectric constant is 7.0 for silicon nitride and between 3.9 and 7.0 for silicon oxynitride depending on its oxygen-nitrogen composition [9], we assumed $C_{fw-surf}$ to be 30fF. To compute $C_{ring-surf}$, we used the metal-1 to substrate capacitance parameters given by MOSIS, assuming that metal-1 to substrate distance is about the same as the distance from metal-3 to the die surface, which is the thickness of the passivation layers deposited on top of metal-3. We multiplied the resulting capacitance value by 6.5/3.9, where 3.9 is the dielectric constant for SiO_2, and 6.5 is our guess for the dielectric constant of the passivation layer that consists of a 0.60μ nitride and a 0.35μ oxynitride film. The resulting capacitance value is 16926fF from the whole Vdd-ring to the die surface.

The orientation of transistor 8 is similar to the one in Figure 4.1, with 85μ by 300μ replaced by 355μ by 135μ. Therefore, the bulk of the charge induced over the floating wire is coming from the parallel Vdd-ring wire 135μ away, and the other portions of the Vdd-ring do not have as much contribution. Thus, we took one-fourth of 16926fF, and bumped it up a little bit to account for the proximity of metal-3 to the passivation layer, and used 4400fF for $C_{ring-surf}$.

The Vdd-ring is 1.5mm long on one inner side, so the die surface area enclosed by the Vdd-ring is $1.5*1.5 = 2.25mm^2$. To estimate the capacitance of the die surface to the substrate, we multiplied 2.25 by $10pF/mm^2$, which is the area capacitance parameter from MOSIS for the metal-3 layer, to obtain 22.5pF. The surface to substrate capacitance between the floating wire and the Vdd-ring wire, which is 135μ away, is less than 10% of 22.5pF, because Vdd-ring is 1500μ on one side, and we took this capacitance to be 2000fF. In our HSPICE runs, we used 10 RC stages between the floating wire and the Vdd-ring as shown in Figure 3.1. Therefore, each C_{surf} in Figure 3.1 is one-tenth of 2000fF, which is 200fF. The RC network between the floating wire and the Vdd-ring represents the 135μ surface distance, but more surface area will be receiving induced charge from the Vdd-ring. In order to model this, we added another 10 RC stages to the left of the floating wire in Figure 3.1.

The only parameters left to be set in Figure 3.1 are the value of R_{surf} and the number of RC stages to the right of the Vdd-ring, which model the surface path from the Vdd-ring to the die

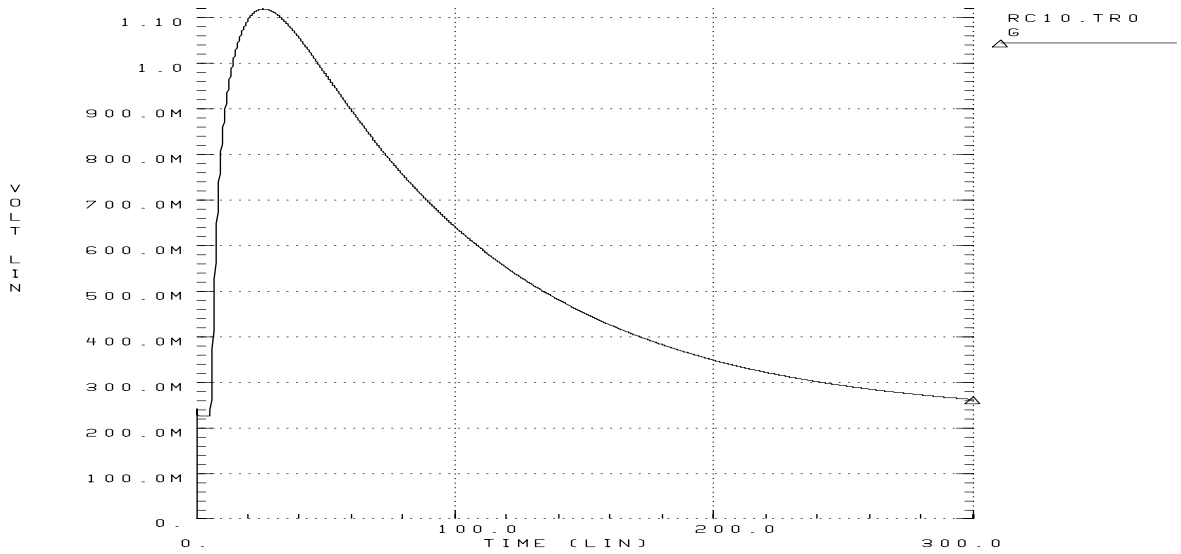

Figure 4.2: The HSPICE simulation showing the Vdd-ring effect through surface conduction

periphery terminating at the substrate. The distance from the Vdd-ring to the outer boundary of a pad cell is 140μ. We expect that the die periphery is pretty close to the outer boundary of a pad cell. Because the 10 RC stages between the floating wire and the Vdd-ring represent a 135μ surface distance, we expect 10 to 20 RC stages to the right of the Vdd-ring in Figure 3.1. Using 15 such RC stages, and setting $R_{surf} = 5 * 10^{11}\Omega$, we obtained the HSPICE simulation result shown in Figure 4.2, which is very close to what we observed experimentally as the "Vdd-ring effect". The y-axis in Figure 4.2 shows the floating wire voltage, and x-axis is time in seconds. The 0.23V at $t = 0$ is obtained by applying 10V to node A in Figure 2.2. At $t = 5sec$, Vdd-ring is switched from 0V to 5V, and stays at 5V throughout the simulation. The RC charge-up takes 20 seconds, and RC discharge is taking more than 275 seconds.

Playing with the value of R_{surf}, we noticed that the amplitude of the RC charge-up does not change with R_{surf}, nor the ratio of RC charge-up time to RC discharge time changes. Only the width of the curve in Figure 4.2 changes. Setting $R_{surf} = 5 * 10^{8}\Omega$ resulted in the simulation result shown in Figure 4.3, which shows that the RC charge-up and discharge cycle completed within half a second after the Vdd-ring is switched to 5V at $t = 5sec$. Half a second would not be a sufficient time for us to see the effect of the Vdd-ring while taking measurements on the taped-lid packages, because we used ordinary digital multimeters. Therefore, air increases the conductivity of the speculated hygroscopic film by a factor of 1000 or more.

4.4 Adsorption by the Die Surface?

More than 40 years ago, Brattain and Bardeen [1] discovered that gas adsorption onto a semiconductor surface changes the conductance of that surface. This is the operating principle for many semiconducting gas and humidity detectors today [11]. It may be possible that either the water molecules themselves or other molecules in the air are adsorbed by the silicon nitride passivation layer, significantly increasing its surface conductivity. When the packages are placed

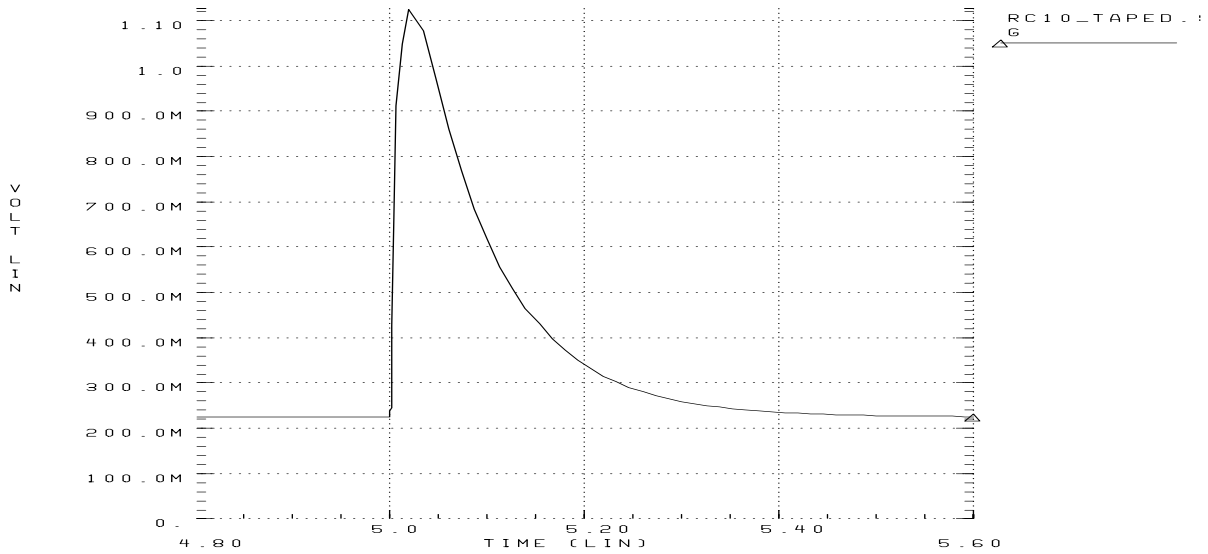

Figure 4.3: The floating wire voltage with $R_{surf} = 5 * 10^8 \Omega$h

in an oven with dry nitrogen passing through, some of the atoms adsorbed from the air may leave the die surface, but still leaving behind enough atoms to cause the surface conduction we have observed. After the packages are sealed with dry nitrogen inside the die cavity, more atoms from the die surface may diffuse into nitrogen very slowly, causing the surface conductivity shift we have observed in 3 months.

The materials used for gas or humidity sensors are semiconductors, but silicon-nitride is an insulator, so we could not find data in the gas sensors literature within our limited time about the adsorption properties of silicon nitride. We are planning to investigate this mechanism in more depth.

4.5 Further Evidence for Our Surface Conduction Model

Further evidence supporting our surface conduction model illustrated by Figure 3.1 is an observation we had during our experiments. Switching the Vdd-ring from 5V back to 0V while the FG voltage is increasing does not stop the increase in FG voltage immediately. The FG voltage continues to increase for a while before it turns back. Our HSPICE simulation showed the same response as illustrated in Figure 4.4. The floating wire voltage continued to increase for 4 seconds after the Vdd-ring voltage is switched to 0V at $t = 12sec$. We used $R_{surf} = 2 * 10^{12}\Omega$ for this simulation mimicing a package with slightly larger hygroscopic film resistivity.

One more evidence for the surface conduction model is the following observation: After setting the pg voltage in Figure 2.1 from 0V to 1.51V for transistor 1, the FG voltage starts from 1.18V, and drops 0.11V to 1.07V after 2.5 minutes. This behavior is due to the time necessary for $C_{fw-surf}$ in Figure 3.1 to increase the potential difference across it by pushing charge into the substrate through the die surface.

Now consider the 135μ surface distance represented by the 10 RC stages in our HSPICE simulations between the floating wire and the Vdd-ring in Figure 3.1. Let's compute the resistance

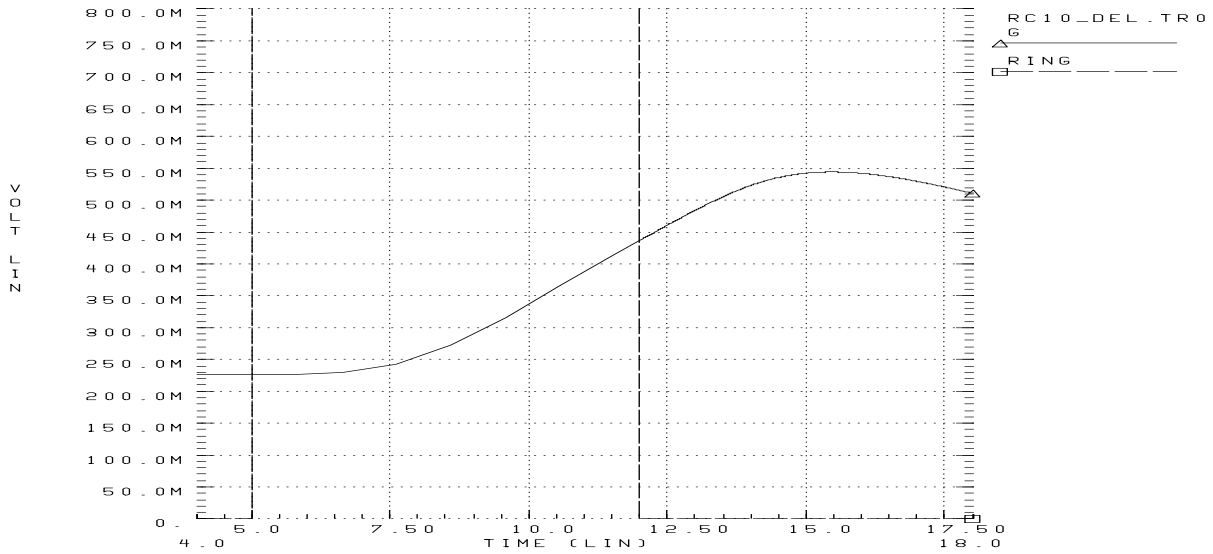

Figure 4.4: The delayed response of the floating wire voltage as another evidence

of this distance through the silicon nitride layer. Let's assume $5 * 10^{13}\Omega - cm$ for the resistivity of the nitride. Then, the resistance $R_{nitride}$ will be

$$R_{nitride} = \frac{resistivity * length}{cross\_section\_area} = \frac{(5 * 10^{13}) * (135 * 10^{-4})}{(0.6 * 10^{-4}) * (1500 * 10^{-4})} = 7.5 * 10^{16}\Omega \qquad (4.1)$$

Since there are 11 R_{surf} resistors in the 10 stage RC network, each R_{surf} will be $7.5 * 10^{16}/11 = 6.8 * 10^{15}\Omega$. Recalling from Section 4.3 that the RC charge-up takes 20 seconds for $R_{surf} = 5 * 10^{11}\Omega$, $R_{surf} = 6.8 * 10^{15}\Omega$ will produce an RC charge-up that takes 272000 seconds, that is 3.15 days! This clearly shows that the silicon nitride is too resistive to be responsible for the Vdd-ring effect.

5. Charge Measurement Results

Figures 5.1 through 5.3 show our trapped charge voltage measurements on 8 taped-lid and 9 hermetically sealed packages. In Figure 5.1, the {42 - taped} column shows the trapped charge voltages in our taped-lid packages for transistors 4 and 10 in Table 2.1, which have 42μ poly extension. Similarly, {42 - sealed} column is for transistors 4 and 10 in our sealed packages. One main conclusion from our measurements is that floating gate transistors with no or some poly extensions have negative trapped charge voltages sitting on their gates, up to almost -4V. This is in contrast with Johnson's measurements [5], who measured always positive charge on his floating gate transistors, which also had some or no poly extensions. This clearly shows the fabrication process dependence of the trapped charge polarity.

Figures 5.2 and 5.3 show that the polarity of the trapped charge can be both negative and positive when a metal wire is connected to a floating gate. Also, the magnitude of V_{tc} is smaller compared to the poly-only case in Figure 5.1. In Figure 5.2, the sealed packages display a trend of larger V_{tc} as the metal layer number increases. But, we believe that this is due to the capacitive coupling of the floating wire through the die surface to other signals in our chip, as shown in Figure 3.1 for the coupling between the Vdd-ring and the floating wire. This trend is not visible for the taped packages in Figure 5.2, and recall that the Vdd-ring effect does not exist for the taped packages. The substrate capacitance of the 250μ floating metal wire is 34fF, 23fF, and 24fF for metal-1, metal-2, and metal-3 layers, respectively. Considering these capacitance values, Figure 5.2 does not show any significant difference in the amount of charge deposited on different metal layers.

In Figure 5.3, the V_{tc} values for the 500μ and 250μ floating wires are not present for the taped packages, because the FG transistors these wires are connected to did not conduct until V_{pg} in Figure 2.1 was around 12V, and the current steadily decreased even though all other voltages were

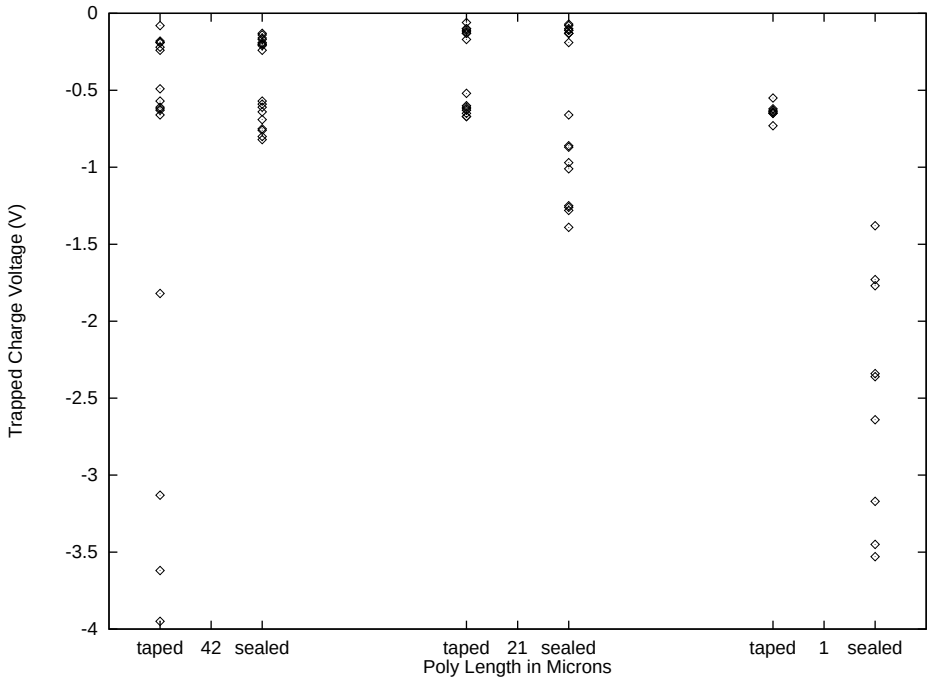

Figure 5.1: V_{tc} with different lengths of poly extensions

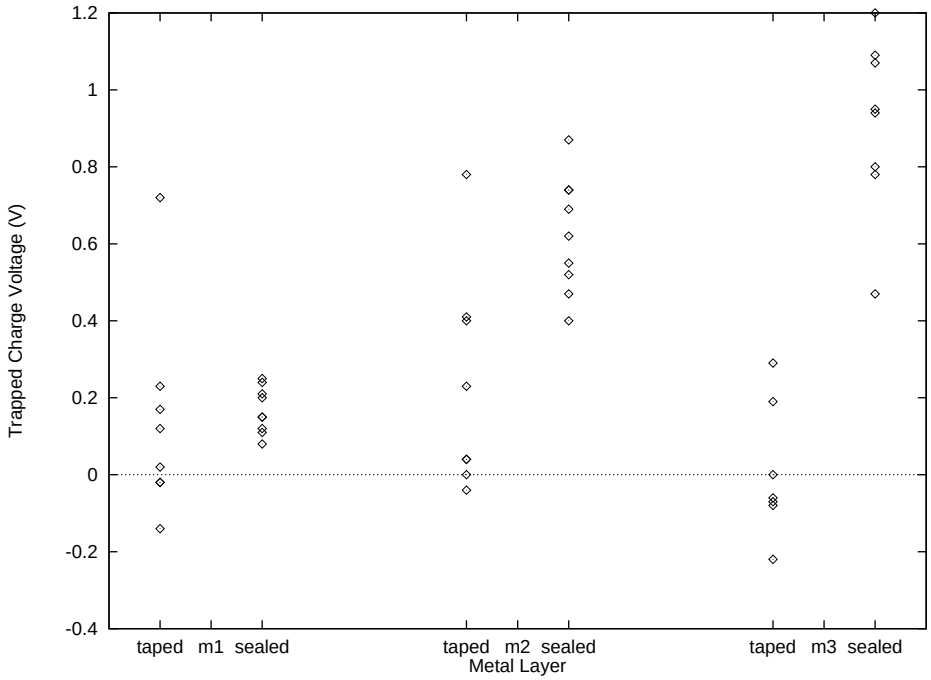

Figure 5.2: V_{tc} with floating wires at different metal layers

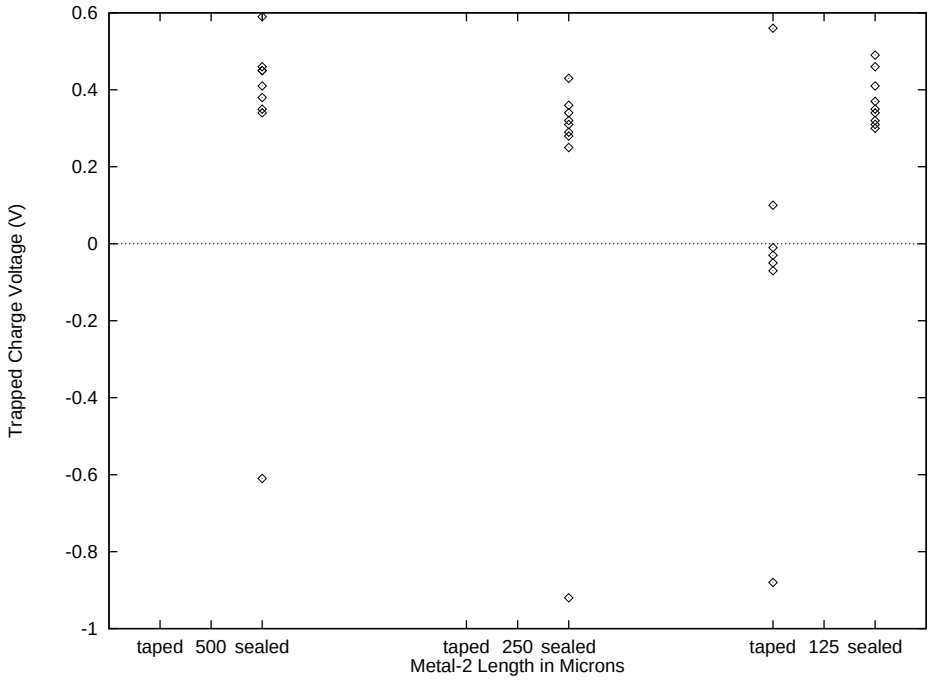

Figure 5.3: V_{tc} with different lengths of floating metal-2 wires

kept fixed. On the other hand, the same FG transistors in the sealed packages started conducting with V_{pg} around 1V, and were stable. We have not explained this behavior, yet. The V_{tc} distribution in Figure 5.3 shows that there is no noticeable change in the amount of charge deposited per unit length of a metal-2 wire as its total length changes.

We exposed some taped packages to ultraviolet light using an EPROM eraser. The trapped charge leaked away, but we noticed that the discharge rate becomes very slow when V_{tc} is low. For instance, reducing V_{tc} from -0.22V to -0.18V for transistor 4 in Table 2.1 took 1 hour of ultraviolet exposure in an EPROM eraser. Therefore, it may not be feasible to zero the trapped charge during fabrication using ultraviolet light.

6. Conclusion

In this paper, we presented experimental evidence that the die surface can act as an RC interconnect capacitively coupling a floating wire to all other signals in a chip. The resistance range for the die surface necessary for this effect is large enough so that the die surface is a perfect insulator for the fault-free operation of the chip. We presented a circuit model for the RC interconnect effect of the die surface. HSPICE simulations with this circuit model produced the same floating-wire behavior we have observed in our experiments. Our experiments and HSPICE simulations show that the passivation layer or the nitrogen gas inside the die cavity is too resistive to cause the die surface act as an RC interconnect. There are two other potential candidates to explain the reduced die surface conductivity. One is a hygroscopic contaminant on the die surface that may form during the time period from the wafers are fabricated to they are cut and packaged. The other is adsorption of water molecules or some other molecules from air by the passivation layer surface. Further study is necessary to identify the actual mechanism.

We have also presented trapped charge voltage measurements on floating-gate transistors with poly or metal extensions. Floating gates with poly extensions always showed negative trapped charge values, up to -4V. Floating gates with metal extensions showed both positive and negative trapped charge values within the -1V to 1V range.

Appendix A.

A.1 Extrapolation Errors

Equation 2.1 in Section 2 is used to compute the trapped charge voltage for transistors 1–5 in Table 2.1 by extrapolating to $V_{pg} = 0$. The value of $K2$ is the largest for transistor 5, because C_{pg-fw} and C_{fw} are the smallest compared to transistors 1–4. From the parameters supplied by MOSIS, we computed both C_{pg-fw} and C_{fw} to be 3fF. Performing an HSPICE simulation with $V_{pg} = 0$, $V_{ds} = 0.2V$, and $V_{tc} = 0$, we found $V_g = K2 * V_{ds} = 15mV$, which is a negligibly small number. This number is even smaller for transistors 1–4.

Again with transistor 5, by varying V_{pg} from 0V to 5V in our HSPICE simulation, $K1 = 0.27$ until V_g reaches the threshold voltage, and $K1 = 0.24$ afterwards. The measurement technique in Figures 2.1 needs the FG transistor be conducting in order to be able to make FG voltage measurements. So, we can only measure FG voltages larger than the threshold value. Using two points computed by HSPICE, $(V_{pg} = 3.75V, V_g = 1.00V)$ and $(V_{pg} = 5.00V, V_g = 1.29V)$ while the transistor is on, extrapolating to $V_{pg} = 0$ results in $V_g = 0.13V$, which is the *extrapolation error*. The reason for the decrease in $K1$ is the decrease in C_{gate} from the cut-off region to the linear region. The extrapolation error decreases as C_{pg-fw} and C_{fw} become larger going from transistor 5 towards 1. Recall that all the transistors in our test chip have the same dimensions: 5.0μ wide and 0.8μ long.

Equation 2.2 is used to compute the trapped charge voltage for transistors 7–12. According to our HSPICE simulations, the value of $K3$ increases from the cut-off region to the saturation region where the FG transistor of Figure 2.2 operates when it is on. This increase in $K3$, caused by the change in the three transistor capacitances C_{gd}, C_{gs}, and C_{gb}, creates a negative extrapolation error. HSPICE simulation with $V_{tc} = 0$ and $C_{fw} = 0.5$fF corresponding to transistor 12 gave us an extrapolation error of -0.47V. We could not use $C_{fw} = 0$, because the transistor did not conduct even when $V_{source} = 5V$ with $C_{fw} = 0$. The extrapolation error with $C_{fw} = 34$fF corresponding to transistor 7 with the largest C_{fw} among transistors 7–12 was -0.07V. Therefore, we expect the extrapolation error for transistors 8–11 to be between -0.5V and -0.07V.

Even though Johnson [5] has not reported his extrapolation errors, we expect his to be similar as ours.

A.2 Advantages of Our Measurement Technique

Controlling the FG voltage with a pg terminal, and keeping the drain-source voltage fixed at 0.2V as shown in Figure 2.1 ensures that the FG transistor will be in the linear region while taking measurements, whereas controlling the FG voltage with the source or drain terminal of the FG transistor, as also done by Johnson [5], allows the transistor to be only in the saturation region while taking measurements, unless there is a large enough V_{tc} on the gate. When an n-channel transistor is in the saturation region, hot electrons can be easily injected into the gate oxide, altering the amount of the trapped charge sitting on the transistor gate. In our setup in Figure 2.1, electrons crossing the channel do not have enough energy to penetrate the gate-oxide. This is the main advantage of this setup. The other advantage is to have pg as an independent terminal to control the FG voltage, without relying on the drain or source voltage.

The p-channel transistors are not as susceptible to hot carrier effect as the n-channel transistors are, so controlling the FG voltage with the source terminal is safe for p-channel transistors.

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