A Novel Dimension Reduction Technique for 3D Capacitance Extraction of VLSI Interconnects

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ABSTRACT

In this paper, a new method named Dimension Reduction Technique (DRT) is presented for capacitance extraction of 3D multilayer and multiconductor interconnects. In this technique, a complex 3D problem is decomposed to a series of simpler 2D problems. Therefore, it results in dramatical savings in computing time and memory usage. Compared to FASTCAP, a field solver based on BEM with multipole acceleration and developed from MIT[NW92], DRT is generally an order of magnitude faster with significantly less memory usage. Based on this technique, accurate close-form formulae or data base can be generated efficiently for calculating the capacitances of some typical 3D structures of VLSI interconnect.

Keywords: interconnects, dimension reduction, field solver library

Figure 1: Hierarchical design procedure of VLSI with incorporation of parameter extraction based on field solver

1 Introduction

Analysis and design of interconnects in high speed VLSI chips, multi-chip modules (MCM's), printed circuit boards (PCB's) and backplanes are gaining importance due to the rapid increase in operating frequencies and decrease in feature sizes. For high speed and high density interconnects, we have to consider the propagation delay and transmission line impedance, together with other effects such as signal degradation caused by transmission line dispersion, signal reflection at discontinuities, crosstalk between adjacent and cross lines, and simultaneous switching noise due to the inductance in power distribution system. Therefore, it is necessary to develop accurate and fast methods to extract the parameters of the interconnects.

The design procedure of a VLSI system is shown in Fig.1. In traditional design process, the approximate formulae are used to calculate the parasitic parameters of layout. With the rapid increase in operating frequencies and decrease in feature sizes, interconnects dominates the system performance. For $0.25\mu m$ design, parameters extraction must be based on a 3D field solver.

Recent years, many methods based on electromagnetc field theory have been applied to parameter extraction of VLSI interconnect. They can be generally classified into two categories. One

category is to solve differential Maxwell equations such as Finite Element method (FEM)[Coa87], Finite Difference method(FDM)[Zem88], and Geometry Independent Measured Equation of Invariance(GIMEI)[HSD96]. They basically divide the space surrounding the object into meshes, then write local equations at each mesh point, which leads to a sparse matrix system. But the standard FD(or FE) method involves large number of unknowns since their truncated boundary conditions are usually valid only far from the object. The other category is to solve electric potential or electromagnetc field integral equations such as Method of Moments(MoM)[CHMS84], the Boundary Element Method (BEM)[PWG92], and the multipole accelerated technique[NW92]. They make meshes on the surface of the object. For multilayer multiconductor interconnects, this means the surface of each conductor and dielectric interface are divided into meshes. Compared to FD, this greatly reduces the number of unknowns. But each small piece is either source or field point, and affected by all others, which leads to a full matrix. Therefore, all these methods will either solve a sparse but very large matrix or solve a small but full matrix.

For 3D interconnects, the number of unknowns in FEM or FDM is proportional to the multiplication of the numbers of mesh nodes in three directions. So, hundreds mesh nodes in each direction will result in millions unknowns. Though the compressed storage technique and some special solvers may be applied to a sparse linear system, it is still time consuming and needs huge memory. Memory size and computing time are the instinct problems for MoM and BEM even with multipole acceleration.

In this paper, we propose a novel dimension reduction technique for 3D structures of VLSI interconnects. We transform the complex 3D problem into a series of 2D problems by decomposing the 3D multilayer and multiconductor interconnect structure into slices. For each slice, we may choose the most effective method to deal with the 2D problem. For instance, in a pure homogeneous dielectric slice, we can get the rigorous analytical solution. Since each slice is homogeneous along the normal direction, the solution is analytical expressions along the normal direction. This means we need not pay additional effort for a 3D interconnect structure with very thin and very thick layers. This results in dramatical savings in computing time and memory needs. For considerable complex 3D multilayer and multiconductor problems, this technique is generally several even tens times faster than the BEM with multipole acceleration (compared with FASTCAP from MIT[NW92]). Based on this technique, accurate close-form formulae or data base can be fast generated for calculating the capacitances of various kinds of 3D interconnects.

2 Interconnect Layout Partition

Fig.2 shows a simple example of interconnect layout, the interconnects in the whole chip will be cut into a large number of elements, which are classified into a number of typical structures, such as those shown in Fig.3. Our goal is to build an accurate and fast field solver library for these typical structures. For a given technology, the most structure parameters, such as the number of layers, permittivities and the thicknesses etc., are given, thus accurate closed-form formulae or data base for typical interconnect structures can be produced based on the field solver library.

Figure 3: Some typical interconnect structures

Figure 4: An example of decomposing multilayer and multiconductor 3D interconnect into slices

3 Dimension Reduction Technique for Capacitance Extraction of 3D Interconnects

A typical 3D multilayer and multiconductor interconnect structure is shown in Fig.4. Based on our dimension reduction concept, this 3D structure may be decomposed into slices as shown in Fig.4.

In ith slice, the potential function ϕ_i satisfies the following 3D Laplace equation

$$\frac{\partial^2 \phi_i}{\partial x^2} + \frac{\partial^2 \phi_i}{\partial y^2} + \frac{\partial^2 \phi_i}{\partial z^2} = 0 \tag{1}$$

Since in each slice, the structure is homogeneous in z-direction, the potential ϕ_i can be expended as

$$\phi_i(x, y, z) = \sum_n [A_{in} \cosh(\alpha_{in} z) + B_{in} \sinh(\alpha_{in} z)] \psi_{in}(x, y) \tag{2}$$

where $\psi_{in}(x,y)$ are called mode functions, and satisfy the following 2D Helmholtz's equation

$$\frac{\partial^2\psi_i}{\partial x^2}+\frac{\partial^2\psi_i}{\partial y^2}+\alpha_i^2\psi_i=0 \tag{3}$$

According to the features of different structure, we may choose different methods to solve the 2D Helmholtz's equation 3.

3.1 Pure Dielectric Layer

In the pure dielectric layer (as the first and fifth layer shown in Fig.4), the solution of Eq.3 can be obtained analytically as

$$\psi_i(x,y)=\sqrt{\frac{\epsilon_p\epsilon_q}{ab}}\cos\frac{p\pi x}{a}\sin\frac{q\pi y}{b}, \qquad p,q=0,1,2,\cdots\cdots \tag{4}$$

where

$$\epsilon_p=\begin{cases}1 & p=0\\ 2 & p>0\end{cases} \qquad \epsilon_q=\begin{cases}1 & q=0\\ 2 & q>0\end{cases} \tag{5}$$

and

$$\alpha_i=\sqrt{(\frac{p\pi}{a})^2+(\frac{q\pi}{b})^2}, \qquad p,q=0,1,2,\cdots\cdots \tag{6}$$

where a and b are the truncated lengths in x and y directions respectively. They should be large enough that the truncated planes may be considered as magnetic walls.

3.2 A 1×1 Cross Over Formulation

Fig.5 is the structure of a 1×1 crossover immersed in five dielectric layers with two parallel ground planes, which is a component cut from a layout shown in Fig.3(b). Here, due to the symmetry of the structure, only one-forth of the structure is considered, and a and b are chosen to be large enough to truncate the two lines and treat the boundary as magnetic wall as shown in the figure.

Because of the regular shape and homogeneous boundary conditions, we can write the mode functions at the five regions analytically. The mode functions in regions Ω_1, Ω_3, and Ω_5 are already given in the above subsection.

In region Ω_2, we have

$$\psi_i(x,y)=\sqrt{\frac{2\epsilon_p}{a(b-b_1)}}\cos\frac{p\pi x}{a}\sin\frac{(q+0.5)\pi(y-b_1)}{b-b_1}, \qquad p,q=0,1,2,\cdots\cdots \tag{7}$$

where ϵ_p has the same meaning as Eq.5, and

$$\alpha_i^2=\sqrt{(\frac{p\pi}{a})^2+(\frac{(q+0.5)\pi}{b-b_1})^2}, \qquad p,q=0,1,2,\cdots\cdots \tag{8}$$

Figure 5: Structure of a 1×1 crossover

And in region Ω_4, we have

$$\psi_i(x,y) = \sqrt{\frac{2\epsilon_q}{(a-a_1)b}} \sin\frac{(p+0.5)\pi(x-a_1)}{a-a_1} \cos\frac{q\pi y}{b}, \qquad p,q = 0,1,2,\cdots\cdots \tag{9}$$

where ϵ_q has the same meaning as Eq.5, and

$$\alpha_i^4 = \sqrt{(\frac{(p+0.5)\pi}{a-a_1})^2 + (\frac{q\pi}{b})^2}, \qquad p,q = 0,1,2,\cdots\cdots \tag{10}$$

After obtaining all the mode functions in the five layers, we can substitute them into Eq.2 with some proper normalization, and transform the problem of finding the potential distribution into finding the corresponding unknown coefficients.

Figure 6: A typical slice and the FD mesh

We then match the potentials at each layer interface which is just a continuous boundary condition: (i) the potential should be continuous at both sides of the interface, (ii) the normal derivative of the potential should also be continuous. Note that the potential equals to either zero in regions where conductor exists, or 1 if there is voltage impressed on this conductor. By making inner product to both sides of the continuous boundary conditions, we can extract the unknown coefficients utilizing the orthogonal property of modes and build a system of linear algebra equations. Because in Eq.2 there are two unknown coefficients A_{in} and B_{in}, the number of equations is the same as the number of unknown coefficients. Solving the linear algebra equations, we can obtain those coefficients, and substitute them into Eq.2, we can finally get the potential distribution.

3.3 More General Cases

An example of a general slice is shown in Fig.6, we can choose suitable numerical methods to solve the 2D Eq.3. For example, we can use FD method to solve it. The FD mesh is also shown in Fig.5. After writing out the FD equations at all mesh nodes, the following eigenvalue equation is obtained as

$$[S]\phi = \lambda\phi \tag{11}$$

where $\lambda = \alpha^2$ is eigenvalue, ϕ the vector consists of the potential values at all mesh nodes, and $[S]$ the sparse matrix resulted from the FD equations at mesh nodes. This equation can be solved with some standard subroutines such as Lanczos method. After the eigenvalues and eigenvectors (discrete mode functions) are obtained, substitute them into Eq.2 and the general solution of

Conductor size in m	FASTCAP C_{11}	DRT C_{11}	difference percent	FASTCAP C_{12}	DRT C_{12}	difference percent
$1 \times 1 \times 5$	1044	1010	3.4%	-229.28	-229	0.1%
$1 \times 1 \times 6$	1197	1163	2.9%	-248	-247	0.4%
$1 \times 1 \times 7$	1314	1308	0.5%	-243.91	-256	4.7%
$1 \times 1 \times 8$	1482	1447	2.4%	-250.3	-261	4.2%
$1 \times 1 \times 9$	1618	1588	1.9%	-265.2	-266	0.3%
$1 \times 1 \times 10$	1794	1729	3.7%	-266	-270	1.5%

Table 1: The comparison of capacitances in pF for crossover interconnect structure

Conductor size	FASTCAP CPU time	DRT CPU time	CPU time $\frac{FASTCAP}{DRT}$	FASTCAP memory	DRT memory	Memory Use $\frac{FASTCAP}{DRT}$
$1 \times 1 \times 5$	28.4	1.0	28.4	24.8	0.9	27.5
$1 \times 1 \times 6$	56.4	1.0	56.4	50	0.9	55.6
$1 \times 1 \times 7$	70.2	1.0	70.2	60	0.9	66.7
$1 \times 1 \times 8$	83.9	2.0	42	70	1.45	48.3
$1 \times 1 \times 9$	102.83	2.4	42.8	77	1.7	45.3
$1 \times 1 \times 10$	133.53	2.4	55.6	106	1.7	62.3

Table 2: Comparison of CPU time in sec. and memory in MB for crossover problem

potential functions are then transformed into the solution of those unknown coefficients. Finally, matching the potential functions at the interfaces between the slices results in a set of matrix equations. The potential distribution functions and then the capacitances are obtained from the solutions of these matrix equations.

4 Experimental Results

Table 1 shows the comparison of the capacitances, and Table 2 shows the computing time and memory usage between DRT and FASTCAP from MIT[NW92] for the crossover structure as shown in Fig.3(b). There are ground planes both at the top and the bottom of the crossover. Here the number of layers is five, the thicknesses of the five layers are chosen to be the same as 1 meter, both the widths of the two conductors are chosen as 1 meter, and the permittivities of the five layers are also chosen the same value 3.9, the lengths of the two conductors are the same and considered as the variable in Table 1 and 2.

It can be seen that the deviations of the capacitances between the DRT and that obtained from FASTCAP are less than 5%, but DRT is tens of times fast than FASTCAP, and the memory use of DRT is far less than that of FASTCAP.

Table 3 4 shows the comparison of the capacitances, computing time and memory needs for a basic structure as shown in Fig.7. It can be seen DRT are about 5% less than the results from the closed-form formula [ST83], and for this simple problem our method is also much fast than FASTCAP. Here, the permittivity is 3.9, the hight of the conductor over the ground plane is 1, the thickness and the width of the conductor are chosen to be 0.5 meter and 1 meter, respectively.

pre-computed parasitics. The best choice for on-line design is to have closed-form expression of corresponding parasitics.

There do exist empirical closed form expression for some interconnection structures, which were mostly obtained from curve fitting of approximate solutions of theoretical analysis or measurements. For the same component, there may be several empirical expressions obtained from different approximations, and each has different valid range. It was also observed that solutions from different approximations could differ considerably [KC79]. Therefore, results from DRT can be used to verify and modify various approximations and empirical expressions which have been developed throughout the last several decades, and can also be used to synthesize closed-form formula of electrical parameters as function of geometry parameters such as widths and spacings.

A simple example of the same structure as in Fig.7 is presented. The following closed-form formula is less than 0.1 percent different from the original calculated results.

$$C = 102 + 191.170635l - 21.9166667l^2 + 2.4722222l^3 - 0.09375l^4 \tag{12}$$

where l stands for the length of the conductor.

6 Conclusion

In this paper, we proposed a novel dimension reduction technique (DRT) which decompose a complex 3D problem into a series of 2D problems. Based on this technique, the capacitance of complex 3D multilayer multiconductor interconnect can be fast and accurately extracted. Some numerical examples show that this technique is generally an order of magnitude faster than FASTCAP, BEM with multipole acceleration, and uses considerably less memory. Based on this technique, we can conveniently generate accurate closed-form formulae which are faster and more convenient for 3D parameter extraction.

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