Pin Assignment and Routing on a Single-Layer Pin Grid Array

Man-fai Yu
Wayne Wei-Ming Dai

UCSC-CRL-95-15
February 24, 1995

Board of Studies in Computer Engineering
University of California, Santa Cruz
Santa Cruz, CA 95064
Phone: +1 (408) 459-4954 or +1 (408) 459-4234
Fax: +1 (408) 459-4829
e-mail: yumf@cse.ucsc.edu or dai@cse.ucsc.edu

ABSTRACT

This paper look at the problem of assigning pins and generating a planar topological routing for a pin grid array package. There is a freedom of assigning any pin to any pad but the routing resource is more limited. We showed that a **monotonic pin assignment** has no detours and has one and only one **monotonic topological routing**. We proposed an algorithm (EVENPGA) that generates this type of topological routing. In addition, EVENPGA creates the optimal uniform distribution of wires and shortest wire length possible for **all** wires under the taxicab wiring metric. If the topological routing is routable, the maximum density of critical cuts along a ring is the minimum theoretically possible. Once the topological routing is done, physical layout can easily be obtained using Surf, a rubberband-based routing system.

Keywords: package routing, pin grid array, planar routing, routability, even wiring
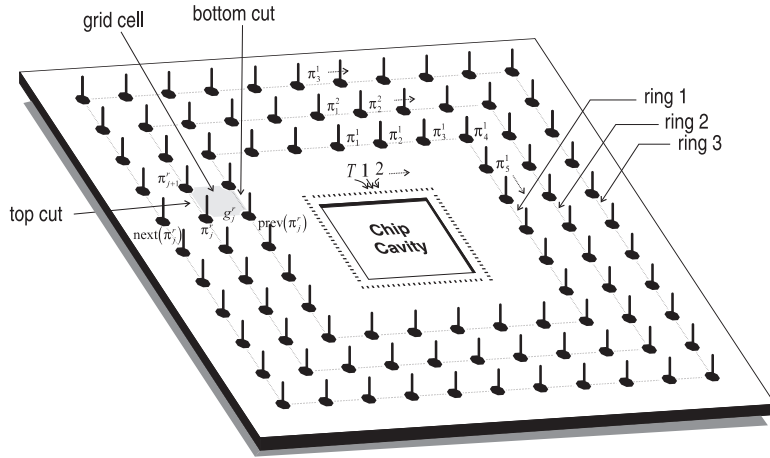
Figure 1: A Conceptual Single-layer PGA Package

1 Introduction

A single-layer pin grid array (PGA) package contains a chip cavity with a single row of wire-bond pads and a rectangular array of pins (Figure 1). At present, most PGA routing is done manually. As the I/O pin count increases, routing a PGA becomes a non-trivial task. In this paper we consider the relationship of pin assignment and routing of a single-layer PGA package. This routing problem is different from general area routing problem in several ways:

- There is no netlist. Each bond pad needs to be routed to one and only one pin. All pins are equivalent.

- The routing pattern is highly symmetric. The pins are on a grid with uniform pitch. The whole package is symmetrical.

- The wires may be routed in all angles.

This paper is the first to consider pin assignment in a package routing. The algorithms proposed in this paper guarantee a planar routing with the most uniform distribution of wires and shortest wire length in the taxicab wiring metric[1]. Previous work by Ying and Gu[2] and Tsai and Chen[3] require an input netlist. Both approaches uses the technique of iterative improvement. Our algorithm creates a topological routing directly and with optimal wire distribution. The only previous work on package routing that considers pin assignment is by Darnauer and Dai[4].

We start with the proof of an important theorem that relates a monotonic pin assignment to a monotonic topological routing. This theorem is the cornerstone of the routing algorithm. Next we present the routing algorithm which generates a monotonic topological routing. The rest of the paper analyzed the properties of the topological routing created by the routing algorithm. The two important results are uniform distribution of wiring and shortest wire length. Since a lot of work has been done on transforming a topological routing into geometric routing. The focus of this paper is on creating a topological routing with desired characteristics.

The Surf routing system[5] is built on the theory developed by Maley[1]. The algorithms presented in this paper is implemented as a topological router within Surf. The transformation of topological routing to detailed routing is done by algorithms proposed by Dai, Dayan and Staepelaere[6]. The design rule enforcement and routability check is done by the algorithms proposed by Dai, Kong and Sato[7].

2   Monotonic Pin Assignment

In this section we present a proof of a theorem that relates a monotonic pin assignment with a monotonic topological routing. We show that a monotonic topological routing is unique for each monotonic pin assignment.

Assume a PGA package has T pads $X = \{1, 2, \ldots, T\}$ arranged in a clockwise manner starting at the center of an arbitrary side of the chip cavity (see Figure 1). The package also has R pin rings $\Pi = \cup_{r=1}^{R} \Pi^r$, where each ring r consists of P_r pins $\Pi^r = \{\pi_1^r, \pi_2^r, \ldots, \pi_{P_r}^r\}$. Since the pins are arranged in rings, all arithmetic involving the subscript of a pin should be modulo P_r. To simplify the mathematics, we assume that the number of pins of innermost ring, ring 1, is divisible by 8. If the number of pins in ring 1 is $8N$, we have

$$T = 4R(2N + R - 1),$$

and

$$P_r = 8(N + R - 1).$$

The problem of routing a single-layer PGA (1LPGA) can be defined as follows:

Problem 1 (1LPGA): *The* single-layer pin grid array routing (1LPGA) *problem is to create detailed routing given the set of pins* Π *and the set of pads* X *in such a way that*

1. *no routing is allowed within the bounding box (chip cavity) of the pads,*

2. *each pad is to be connected to one and only one pin.*

1LPGA assumes that the number of pads and pins are the same so that connections has to be made for all pins, i.e. $|\Pi| = |X|$. To solve 1LPGA, we divide the process into three steps.

1. Pin assignment.

2. Topological Routing.

3. Detail Routing.

First we start with a formal definition of a pin assignment.

Definition 1: *A* pin assignment *is a one-to-one and onto mapping* $\Phi : \Pi \rightarrow X$.

Definition 2: *A* monotonic topological routing (MTR) *is a topological routing such that all wires* $w = (\pi_j^r, p)$ *satisfy the following conditions:*

1. **Detour Condition** *intersect at most one cut* (π_k^s, π_{k+1}^s) *for some* k *in all the rings* s, *and*

2. **Chip Cavity Condition** *does not intersect cuts* $(q, q+1)$ *for all* $q \in X$, *and*

3. **Shortest Path Condition** *is shortest between pad* p *and the cut on ring 1 that intersects* w, *i.e. the cut* (π_k^1, π_{k+1}^1) *where* $\Phi(\pi_k^1) < p < \Phi(\pi_{k+1}^1)$. *If* w *is a connection between* p *and a pin in ring 1, then* w *is the shortest path between the pad and the pin.*

The detour condition means that all wires originate from the bond pads fan out towards the periphery without taking any detours. Once a wire is outside a ring, it does not reenter it. The chip cavity condition ensures that there is no wiring in the chip cavity. The shortest path condition prevents the wire from routing around the whole chip cavity before intersecting ring 1 or connecting to a pin in ring 1.

MTR is usually the desired routing because the wire length is the shortest possible. We would like to find out the relationship between an MTR and a pin assignment. Specifically, we want to know what kind of pin assignment can guarantee an MTR. We discovered that an MTR will exist and is unique if the pad number assigned to the pins in the same ring strictly increase. We call this specific class of pin assignment *monotonic pin assignment (MPA)*.

Definition 3: *A* monotonic pin assignment (MPA) *is a pin assignment such that for all* r, $\Phi(\pi_i^r) >$ $\Phi(\pi_j^r)$ *if and only if* $i > j$.

Lemma 1: *Given a monotonic pin assignment, a monotonic topological routing exists.*

Proof: We construct the routing as follows: Starting with ring 1, we fanout the wires from the pad frame to the ring using the shortest path possible. The wires are not allowed to enter the chip cavity. If a pad is assigned to a pin in ring 1, then make the connection. Otherwise, place the wire (say from pad p) between the cut of adjacent pins π_i^1 and π_{i+1}^1 where $\Phi(\pi_i^1) < p < \Phi(\pi_{i+1}^1)$ or, if $p > \Phi(\pi_i^1)$ for all i, choose the cut $(\pi_1^1, \pi_{P_r}^1)$. Arrange the wire order in each cut between pairs of pins in ring 1 such that, if the ordering is $(\pi_i^1, w_1, w_2, \ldots, w_n, \pi_{i+1}^1)$, then $\Phi(\text{pinof}(w_i)) < \Phi(\text{pinof}(w_{i+1}))$. Repeat the operation on ring 2, 3, ..., R.

Now we will prove that the topological routing constructed is an MTR. Since the construction is done from inside out ring by ring, a wire $w = (\pi_i^r, p)$ will make the connection to π_i^r in the rth iteration. Each wire only pass through one cut on each ring and does not intersect with the rings above its connecting pin. Hence the detour condition is satisfied.

Consider the whole ring r as a cut. The order of pins and wires is

$$C = (\pi_1^1, w_1, w_2, \ldots, w_n, \pi_2^1, w_{n+1}, \ldots, \pi_3^1, \ldots, \pi_{P_1}^1)$$

To simplify discussion, we define $\Phi(w) = \Phi(\text{pinof}(w))$ where w is a wire. Due to the way we construct the wires, for any two objects ρ_1 and ρ_2, and ρ_1 precedes ρ_2 in the cut C, we have $\Phi(\rho_1) < \Phi(\rho_2)$. This is the same order as the ordering of the pads. Therefore all the wires starting at the pad frame fan to ring 1 with no crossing. This means that the shortest-path algorithm used will not create wires that enter the chip cavity.

Finally, the shortest path from pad to ring 1 for all wires guarantees the shortest path condition. $\square$

In fact, for each MPA, there is only one MTR. This is very useful because now all we need to do is to create an MPA.

Lemma 2: *Given a monotonic pin assignment, there is a unique monotonic topological routing.*

Proof: By contradiction. Suppose there are two MTRs for a given MPA. Then there exists
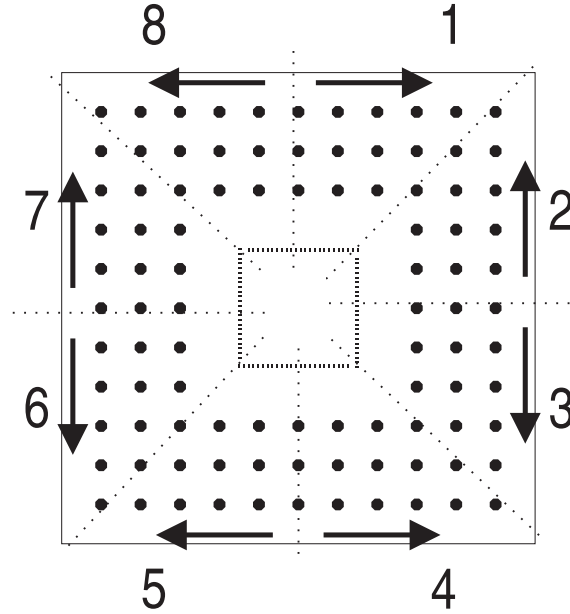
Figure 2: Assignment Directions in Each Sector of a Package

a pin π_i^r such that there are two possible topological routing w_1 and w_2 for the same assignment (π_i^r, p). Since they are topologically different and the routing is an MTR, there exist two pins π_j^s and π_k^t where $s, t < r$, such that exactly one of the wires crosses the cut $c = (\pi_j^s, \pi_k^t)$. Assume without lost of generality that w_1 crosses the cut and $\Phi(\pi_j^s) < \Phi(\pi_k^t)$. Since w_1 crosses c, we have $\Phi(\pi_j^s) < p < \Phi(\pi_k^t)$. Also, since w_2 does not cross c, we have either $p < \Phi(\pi_j^s)$ or $p > \Phi(\pi_k^t)$. This is a contradiction. Hence it is impossible to have two topological routing for an MPA. $\square$

Combining Lemma 1 and Lemma 2, we have:

Theorem 1 (Existence and Uniqueness): *There exists a unique monotonic topological routing for any given monotonic pin assignment.*

The above theorem implies that the problem of generating an MPA is equivalent to the problem of creating an MTR. This immensely simplifies our task because now we can predict the routability of the design without creating the topological routing.

3   Creating an MTR

In this section we present an algorithm that generates a "good" monotonic pin assignment so

Algorithm 1 (EVENPGA):

Algorithm EVENPGA(Set of Pins Π, Ordered set of pads X)

    For rings $r \leftarrow 1$ to R

        Stepsize $k \leftarrow \lfloor |X|/P_r \rfloor$ ...(*)

        Remainder $q \leftarrow |X| - kP_r$

        Pin number $j \leftarrow 1$

        For pads $i \leftarrow 1$ to $|X|/8$

            ASSIGN8$(X[i], j, r)$

            $j \leftarrow j + 1$

            If $i \leq (q/8)(k+1)$

            Then $i \leftarrow i + k + 1$

            Else $i \leftarrow i + k$

        Endfor

        Remove all assigned pads from X

    Endfor

Subroutine ASSIGN8(i, j, r)

    Assign pad i to pin π_j^r (Sector 1)

    Assign pad $|X|/4 - i + 1$ to pin $\pi_{P_r/4-j+1}^r$ (Sector 2)

    Assign pad $|X|/4 + i - 1$ to pin $\pi_{P_r/4+j-1}^r$ (Sector 3)

    Assign pad $|X|/2 - i + 1$ to pin $\pi_{P_r/2-j+1}^r$ (Sector 4)

    Assign pad $|X|/2 + i - 1$ to pin $\pi_{P_r/2+j-1}^r$ (Sector 5)

    Assign pad $3|X|/4 - i + 1$ to pin $\pi_{3P_r/4-j+1}^r$ (Sector 6)

    Assign pad $3|X|/4 + i - 1$ to pin $\pi_{3P_r/4+j-1}^r$ (Sector 7)

    Assign pad $|X| - i + 1$ to pin $\pi_{P_r-j+1}^r$ (Sector 8)

Figure 3: Algorithm EVENPGA

that the wires are distributed as uniformly as possible. Evenly distributed wiring is highly desired in a package design due to routability, performance and technology concerns. A evenly distributed routing is the least congested and the average wire-to-wire distance is also the highest, which means that crosstalk level and yield are both optimized.

The algorithm (Figure 3) takes advantage of the symmetric geometry of the package and divides it into eight sectors. Figure 2 shows the direction of assignment in each sector and the dividing lines.

Since each pad is visited once, EVENPGA runs in order $O(|X|)$. The storage complexity is the size of the output, i.e. $O(|\Phi|) = O(|X|)$.

Algorithm 2 (MAKEMTR):
Algorithm MAKEMTR(Φ, X, Π)
    For $r \leftarrow 1$ to R
        For $i \leftarrow 1$ to P_r
            Route π_i^r to $\Phi(\pi_i^r)$

Figure 4: Algorithm MAKEMTR

Also note that all arithmetics are integer. All divisions have no remainders except the line marked (*). We can observe the following invariants:

- $|U| = P_r$ at the end of i-loop.

- $|X|$ is divisible by 8.

- q is divisible by 8.

It is straightforward to verify that EVENPGA creates an MPA. On every ring, the pins are assigned in increasing or decreasing order. The pads are assigned in the same ordering as the pins. The eight assignments in ASSIGN do not cross each other except at the corners where they give identical assignments.

After the assignment, we can generate the topological routing using the simple algorithm MAKEMTR (Figure 4).

The routing from π_i^r to $\Phi(\pi_i^r)$ is created by the shortest-path algorithm described by Dai, Dayan and Staepelaere[6]. After the topological routing is created, design rules can be enforced as proposed by Dai, Kong and Sato[7]. This is based on the rubber-band representation of topological routing as presented by Dai, Kong, Jue and Sato[8].

Since MAKEMTR is correct because the wire length is the shortest possible for all wires. Section 5 analyzed the wire lengths of the routing created by EVENPGA. The time complexity of MAKEMTR is $O(|X|)$.

4 Uniform Wiring Distribution

An important property of EVENPGA is that it distributes the wires as uniformly as possible around the rings. The pin assignment ordered the wiring in such a way that no crossing is necessary. This is a major advancement over previously proposed algorithms[3, 2].
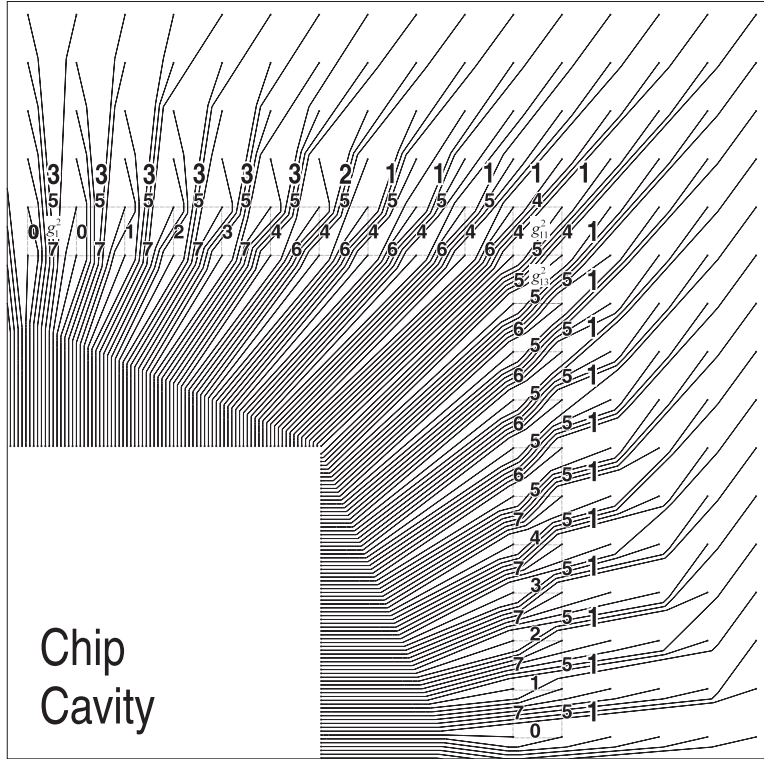
Chip
Cavity

Figure 5: Top Right Quadrant of a PGA Package

To simplify the mathematics, we assume that the pin pitch is 1 unit distance. Let the expression $\text{next}(\pi_i^r)$ denote the pin on ring $r+1$ that is closest to π_i^r. Note that next() is undefined for a corner pin. Similarly, $\text{prev}(\pi_i^r)$ denote the pin on ring $r-1$ that is closest to π_i^r. At a corner, three pins have the same prev()—the corner pin and its two neighbors on the same ring. We define a *grid cell* g_i^r to be the area bounded by the pins π_i^r, π_{i+1}^r, $\text{prev}(\pi_i^r)$ and $\text{prev}(\pi_{i+1}^r)$. π_i^r cannot be a corner pin. If π_{i+1}^r is a corner pin, then the cell is defined by the area bounded by π_i^r, π_{i+1}^r, π_{i+2}^r and $\text{prev}(\pi_i^r)$. Intuitively, π_i^r is at the upper left corner of g_i^r. We define the *bottom cut* of a cell g_i^r to be the cut $(\text{prev}(\pi_i^r), \text{prev}(\pi_{i+1}^r))$, the *top cut* to be (π_i^r, π_{i+1}^r), the *left side cut* to be $(\pi_i^r, \text{prev}(\pi_i^r))$ and the *right side cut* to be $(\pi_{i+1}^r, \text{prev}(\pi_{i+1}^r))$. Figure 1 shows a pin π_i^r, $\text{next}(\pi_i^r)$, $\text{prev}(\pi_i^r)$ and the grid cell g_i^r.

Now we proceed to prove that EVENPGA produces a uniformly distributed topological routing. The following lemma states that the wires are uniformly distributed among the cuts in all the rings. More precisely, it says that the number of wires between two adjacent pins in the same ring differs

at most by one.

Lemma 3: *For all $r = 1, \ldots, R$,*

$$\max_{\forall i}(F(\pi_i^r, \pi_{i+1}^r)) - \min_{\forall i}(F(\pi_i^r, \pi_{i+1}^r)) \leq 1.$$

$F(\pi_i^r, \pi_j^s)$ is the flow of the cut (π_i^r, π_j^s), i.e. the number of wires intersecting the cut.

Proof: By induction on r. For ring 1, in each iteration of i, it is incremented by either k or $k + 1$. Hence the number of wires between any two adjacent pin in ring 1 is either $k - 1$ or k. Therefore

$$\max_{\forall i}(F(\pi_i^r, \pi_{i+1}^r)) - \min_{\forall i}(F(\pi_i^r, \pi_{i+1}^r)) \leq k - (k - 1) = 1.$$

Now assume that it is true for rings $1, 2, \ldots, r$. Consider ring $r + 1$. Since the pads assigned to the first r rings are removed from the set X, this is exactly the problem instance (Π', X') where $\Pi' = \cup_{i=r+1}^R \Pi^i$ and $X' = X - $ all assigned pads. By a similar argument as ring 1, it is true for ring $r + 1$. $\square$

Lemma 3 is not strong enough for a uniform wire distribution because the wires may not be even between the rings. We are going to show that this is not the case. Figure 5 shows the top right quadrant with the flows of the cuts in the first ring. At the center of the top side and the right side, the wires intersect the ring at right angles. At the corner, the wires intersect the ring at 45 degrees. Consider the two side cuts of a grid cell at the center, i.e., the cuts $(\pi_i^r, \text{prev}(\pi_i^r))$ and $(\pi_{i+1}^r, \text{prev}(\pi_{i+1}^r))$ for a grid cell g_i^r. All the wires enter at the bottom and leave at the top. There are no wires going through the two side cuts. For a grid cell near the corner, most wires enter at the bottom and leave at one of the sides. There is a transition from zero to many wires as we move from the top center to the top right corner. The inverse transition takes place when we move from the corner to the right center. We want to know how smooth the transition is and the bound of the maximum side flow.

We start with a lemma that relates the step sizes of adjacent rings.

Lemma 4: *Let k_r and k_{r+1} are the values of k in iteration r and $r + 1$ respectively. If $R < \sigma$ then $0 < k_r - k_{r+1} < 3$ where $\sigma = 1/2 - N + \sqrt{3N^2 + 3N + 1/4}$.*

Proof: Let X_r be the set X at iteration r. At iteration r, $|X| = T - 4(r-1)(N + (r-1) - 1) =$

$T - 4(r-1)(N + r - 2)$. From EVENPGA,

$$k_r = \lfloor |X_r|/P_r \rfloor, \quad k_{r+1} = \lfloor |X_{r+1}|/P_{r+1} \rfloor.$$

We have

$$
\begin{aligned}
k_r - k_{r+1} \quad &> \quad \frac{T - 4(r-1)(2N + r - 2)}{8(N + r - 1)} - \frac{T - 4r(2N + r - 1)}{8(N + r)} - 1 \\
&= \quad \frac{4R(2N + R - 1) - 4r(2N + r - 1)}{8(N + r - 1)(N + r)} > 0
\end{aligned}
$$

since $R \geq r$.

$$
\begin{aligned}
k_r - k_{r+1} \quad &< \quad \frac{T - 4(r-1)(2N + r - 2)}{8(N + r - 1)} - \frac{T - 4r(2N + r - 1)}{8(N + r)} + 1 \\
&\leq \quad \frac{R(2N + R - 1) - 2N}{2N(N + 1)} + 2
\end{aligned}
$$

It can be shown that the right hand side is less than 3 if $R < \sigma$. Thus $0 < k_r - k_{r+1} < 3$ if $R < \sigma$. $\square$

Since $\sigma > N/2$ and in most packages R is far less than N, this requirement is not a strong constraint. From now on we will assume that R always satisfy this requirement.

We will now derive a relationship between the step sizes of adjacent rings. Since in each iteration of i, i increments either k or $k + 1$, it appears that the difference of step sizes between two adjacent rings may be as large as 3. The following lemma states that in fact the maximum difference is at most 2. This is because of the relative magnitudes of the remainder q.

Lemma 5: *Let T_i^r be the flow of the top cut of a cell g_i^r and B_i^r be the flow of the bottom cut of the same cell. Then $1 \leq B_i^r - T_i^r \leq 2$ if $R < \sigma$.*

Proof: Since $k_r - 1 \leq T_i^r \leq k_r$ and $k_{r-1} - 1 \leq B_i^r \leq k_{r-1}$, we have $B_i^r - T_i^r \leq k_{r-1} - k_r + 1$. By Lemma4, either $k_{r-1} - k_r = 1$ or $k_{r-1} - k_r = 2$. If $k_{r-1} - k_r = 1$, $B_i^r - T_i^r \leq 2$. Otherwise we have the following equations.

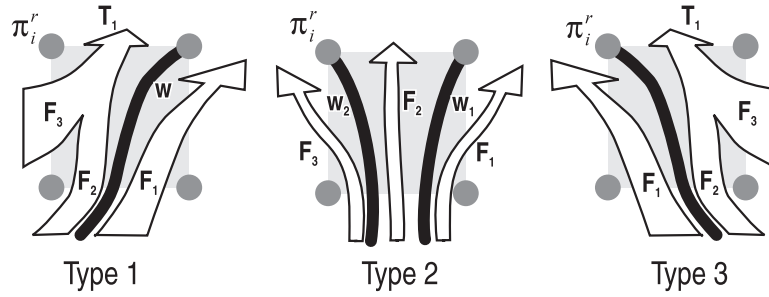$$|X_r| = k_r P_r + q_r, \quad |X_{r-1}| = k_{r-1} P_{r-1} + q_{r-1}.$$

Figure 6: The flows of a grid cell

Solving them, with $k_r - k_{r-1} = 2$, we have $q_r - q_{r-1} = P_{r-1} - 8k_{r-1} + 16$. It can be shown that this is greater than 0 if $R < \sigma$.

On each ring, EVENPGA first make steps of $k + 1$ for q pins and then switch to steps of k. If $q_r > q_{r-1}$, we can divide the i-loop into three regions.

Region I $j \leq q_{r-1}$. In this region $T_i^r = k_r$ and $B_i^r = k_{r-1}$, so $B_i^r - T_i^r = 2$.

Region II $q_{r-1} < j \leq q_r$. In this region $T_i^r = k_r$ and $B_i^r = k_{r-1} - 1$, so $B_i^r - T_i^r = 1$.

Region III $j > q_r$. In this region $T_i^r = k_r - 1$ and $B_i^r = k_{r+1} - 1$, so $B_i^r - T_i^r = 2$.

If $k_{r-1} - k_r = 2$, $B_i^r - T_i^r \geq 1$. Otherwise, solving the same set of equations with $k_r - k_{r-1} = 1$, we have $q_r - q_{r-1} = 8(1 - k_{r-1}) \leq -1$. Hence $q_{r-1} > q_r$ if $k_{r-1} - k_r = 1$. We can also divide the i-loop into three regions.

Region I $j \leq q_r$. In this region $T_i^r = k_r$ and $B_i^r = k_{r-1}$, so $B_i^r - T_i^r = 1$.

Region II $q_r < j \leq q_{r-1}$. In this region $T_i^r = k_r - 1$ and $B_i^r = k_{r-1}$, so $B_i^r - T_i^r = 2$.

Region III $j > q_{r-1}$. In this region $T_i^r = k_r - 1$ and $B_i^r = k_{r-1} - 1$, so $B_i^r - T_i^r = 1$.

Therefore in any case, $1 \leq B_i^r - T_i^r \leq 2$. $\square$

From Lemma 5, we can bound the difference of neighboring side cuts. Let the flow through the left and right side cut of the grid cell g_i^r be L_i^r and R_i^r respectively. If the number of pins connected with a wire in the cell is a, we have the following equation.

$$L_i^r + B_i^r = T_i^r + R_i^r + a \Rightarrow R_i^r - L_i^r + a = B_i^r - T_i^r \tag{4.1}$$

Figure 6 illustrates three types of cells based on the possible flows within the cell. We only

need to investigate the change of cell type along the top center edge towards the top right corner because the package is symmetrical.

We start with the first cell in ring r. Cell g_1^r can be any type. Note that $L_1^r = 0$. Since $B_1^r - T_1^r$ is at most 2, $R_1^r = 0$. $a = 1$ if $B_1^r - T_1^r = 1$ and $a = 2$ otherwise.

Now consider the cell g_i^r and g_{i+1}^r. There are four cases.

Case I g_i^r is Type 3 and $B_{i+1}^r - T_{i+1}^r = 1$. $R_{i+1}^r - L_{i+1}^r = 0$ because $a = 1$ for a Type 3 cell. This means that g_{i+1}^r is also a Type 3 cell.

Case II g_i^r is Type 3 and $B_{i+1}^r - T_{i+1}^r = 2$. Since the left neighbor of g_{i+1}^r is Type 3 and since $L_1^r = 0$ and L_i^r does not change between neighboring Type 3 cells (Case I), $L_{i+1}^r = 0$. Since g_i^r is Type 3, π_{i+1}^r must be connected within $g_{i+1}r$. If $R_{i+1}^r > 0$, then π_{i+2}^r will not be connected because $B_{i+1}^r - T_{i+1}^r - $ Connection of $\pi_{i+1}^r = 1$. It is impossible to connect this pin in the next cell, g_{i+2}^r, because the wire leaving the right side cut will block any possible connection in g_{i+2}^r. Therefore R_{i+1}^r must be 0. g_{i+1}^r is a Type 2 cell.

Case III g_i^r is Type 2. $L_{i+1}^r = 0$ by Case II. Note that π_{i+1}^r is connected within g_i^r. Therefore g_{i+1}^r can only be a Type 1 cell. $R_{i+1}^r - L_{i+1}^r = 1$ if $B_{i+1}^r - T_{i+1}^r = 2$ and $R_{i+1}^r - L_{i+1}^r = 0$ otherwise.

Case IV g_i^r is Type 1. g_{i+1}^r must be a Type 1 cell because π_{i+1}^r is already connected in g_i^r. $R_{i+1}^r - L_{i+1}^r = 1$ if $B_{i+1}^r - T_{i+1}^r = 2$ and $R_{i+1}^r - L_{i+1}^r = 0$ otherwise.

We summarize the cases into the following lemma.

Lemma 6: *The right neighbor of a cell can only be of certain type.*

1. *The right neighbor of a Type 1 cell must be a Type 1 cell.*

2. *The right neighbor of a Type 3 cell can be a Type 3 cell or a Type 2 cell.*

3. *The right neighbor of a Type 2 cell is a Type 1 cell.*

Figure 5 shows the types of cells in the second ring. The chain breaks at the corner cell g_{13}^3. Note that the Type 1 cells on the right edge are mirrored with respect to the one shown in Figure 6 because the upper right edge is assigned in counterclockwise direction from the center of the right edge (Figure 2). In general, if the first cell in the ring is Type 1, then all the cells up to top right corner is Type 1. If the first cell is Type 2, all the cells except the first is Type 1. If the first cell is Type 3, somewhere along the path the chain of Type 3 cells will end with a Type 2 cell (where $B_i^r - T_i^r = 2$) and then after the Type 2 cell everything is Type 1. The cells from the center of right

edge to the top right corner are all Type 1. The chain ends at a corner cell because the orientation of the cells changed.

From all four cases the maximum difference between R_i^r and L_i^r is 1. Therefore we have the following lemma.

Lemma 7: *The change of flow between two neighboring side cuts is at most 1.*

From the four cases we can see that only Type 1 cells can have $R_i^r - L_i^r > 0$. So the maximum flow on side cuts from the top center to the top right corner is less than or equal to the number of Type 1 cells with $B_i^r - T_i^r = 2$. From the proof of Lemma 5, we know that $B_i^r - T_i^r = 2$ happens only in:

1. Region I and III if $q_r > q_{r-1}$ and

2. Region II if $q_{r-1} > q_r$.

If $q_r > q_{r-1}$, the number of cells where $B_i^r - T_i^r = 2$ is equal to $q_{r-1} + (k_{r-1} - q_r) < k_{r-1}$. If $q_{r-1} > q_r$, the number of cells is equal to $q_{r-1} - q_r < k_{r-1}$. Therefore we have the following conclusion.

Lemma 8: *The maximum flow of a side cut between rings r and $r + 1$ is less than k_r.*

Now we have rather tight bounds on the cuts in the rings and on all the side cuts. To show that EVENPGA generates a even wiring distribution, we measure the densest cuts within the grid cells along a ring. We will show that the difference of the densest cuts will not differ by more than 1. Since the cuts within a ring has a uniform density (Lemma 3), the critical cut within a grid cell and its density is determined by the amount of side flow. There are only two competing cuts within the cell that can be the critical cut of the cell—the bottom cut and the diagonal cut which have the larger flow. At the center of an edge, the side flow is 0. All wires enter the cell from the bottom cut and leave from the top cut. The critical cut is between two adjacent pins in the same ring, i.e. (π_1^r, π_2^r). This cut is critical because at least $k_r - 1$ and at most k_r wires intersect it. At a corner cell, wires enter the cell from both the bottom and a side and leaves from the top and the other side. Any one side cut is not as critical because there is only at most k_r wires intersect it. However, the diagonal cut, either $(\pi_i^r, \text{prev}(\pi_{i+1}^r))$ or $(\pi_{i+1}^r, \text{prev}(\pi_i^r))$, become more critical because up to $2(k_r - 1)$ wires may intersect it. These wires include the $k_r - 1$ wires from the bottom cut and up to $k_r - 1$ wires from a side cut (Lemma 8). The densities of the critical cuts of cells from

the top center to the top right corner is bounded by the density of the critical cut of the cell at the center and that at the corner because the amount of side flow increase monotonically from center to corner. Therefore the maximum difference of densities of critical cuts across the ring is the difference of densities of critical cuts between a center cell and a corner cell. The following lemma summarizes the arguments.

Lemma 9: *The critical cuts of ring r is either the bottom cut (π_1^r, π_2^r) or the diagonals $(\pi_{P_r/8}^{r+1}, \mathrm{prev}(\pi_{P_r/8+1}^{r+1}))$ and $(\pi_{P_r/8+1}^{r+1}, \mathrm{prev}(\pi_{P_r/8}^{r+1}))$.*

EVENPGA tries to decrease the density of the diagonal cut at the corners because a diagonal cut does not have twice the capacity of a side cut but may have up to $2(k_r - 1)$ wires intersecting it. It put all the extra wires (there are q of them) at the center.

The optimal wire distribution is such that the maximum difference of densities of the critical cuts in all the cells among a ring is less than 1. Mathematically,

$$\Delta^* = \max_{\forall i}(D(\mathrm{crit}(g_i^r))) - \min_{\forall i}(D(\mathrm{crit}(g_i^r))) < 1$$

$D(c)$ is the density of a cut c and $\mathrm{crit}(g)$ is the critical cut of the grid cell g which is one of the cuts listed in Lemma 9.

We will show that the maximum difference in a routing generated by EVENPGA is *optimal* if $k_r < 3 + 2\sqrt{2} = 5.83$.

Theorem 2 (Even Wiring): *EVENPGA generates a topological routing such that*

$$\Delta = \max_{\forall i}(D(\mathrm{crit}(g_i^r))) - \min_{\forall i}(D(\mathrm{crit}(g_i^r))) < 1$$

if $k_r < 3 + 2\sqrt{2}$.

Proof: By Lemma 9, $\Delta = |D(\text{bottom cut}) - D(\text{diagonal})|$. The density of the bottom cut of the cell in the center of the top edge is k_r. The density of the diagonal cut at the top right corner cell is less than or equal to $2(k_r - 1)$. Hence $\Delta = |2(k_r - 1)/\sqrt{2} - k_r|$. This is less than 1 if $1 < k_r < 3 + 2\sqrt{2}$. □

Since $k_r > k_{r+1}$, Lemma 9 implies that the critical cuts of the whole package is on ring 1.

Finally, we consider whether EVENPGA produces an optimal routing in the sense that the maximum density of any critical cut in any cell in a ring is the minimum. Consider the cuts around ring 1. If we want to minimize the maximum density of the cuts in the ring, i.e. the density of cuts (π_i^1, π_{i+1}^1) for all i, we must spread out the wires evenly among all cuts. Thus the minimum flow for these cuts must be $\lfloor T/8N \rfloor$. With this strategy, the maximum density is $\lceil T/8N \rceil/1 = \lceil T/8N \rceil$. Lemma 3 showed that the maximum difference of flow of an MTR created by EVENPGA is less than or equal to 1. Since $k_1 = \lfloor T/8N \rfloor$, the MTR of EVENPGA exactly equals the minimum and maximum flow requirements. Therefore we have following conclusion.

Theorem 3: *If the MTR created by EVENPGA is routable, the maximum density of the critical cut is the minimum possible.*

5   Wire Length Analysis

Intuitively, the wire length generated by EVENPGA is short. MPA guarantees an MTR which means no detours for any net. In this section, we will derive a bound for the wire length of all nets.

First we find the bound on the number of side, bottom and top cuts of the grid cells a wire may intersect. Let $\Gamma(w)$ be the total number of side, bottom and top cuts of cells w intersected. Since no detouring is allowed by the definition of MTR, a connection $w = (\pi_i^r, p)$ must pass through exactly one cut on ring 1, 2, ..., $r - 1$. So $\Gamma(w) \geq r - 1$ for all w.

Next we will show that a wire intersects at most one side cut between any pair of adjacent rings. To show that this is true, we need the following lemma:

Lemma 10: *A grid cell g_i^r is always one of the three types as shown in Figure 6.*

Proof: From the four cases discussed before Lemma 6, the side flows of Type 2 and Type 3 cells are always 0. For Type 1 cells, the difference of side flows may be 1. In Figure 6, the connection wire is between the flows F_1 and F_2 in a Type 1 cell. For a Type 1 cell g_i^r where $B_i^r - T_i^r = 2$, $L_i^r - R_i^r = 1$ so $F_1 - F_3 = 1$. Consider the right neighbor of this cell g_{i+1}^r. It must be Type 1 (Lemma 6). If $B_{i+1}^r - T_{i+1}^r = 2$ in this cell too, $R_{i+1}^r - Li + 1^r = 1$. So $F_1 = R_{i+1}^r = 1 + L_{i+1}^r = 1 + R_i^r = 2 + L_i^r$. Therefore F_1 monotonically increase down the chain of Type 1 cells. The question is: since the flow of the bottom cut, B_i^r is either k_r or $k_r - 1$, will F_1 be greater than or equal to B_i^r so that at the end of a long chain of Type 1 cells the connecting wire comes from the left side cut instead
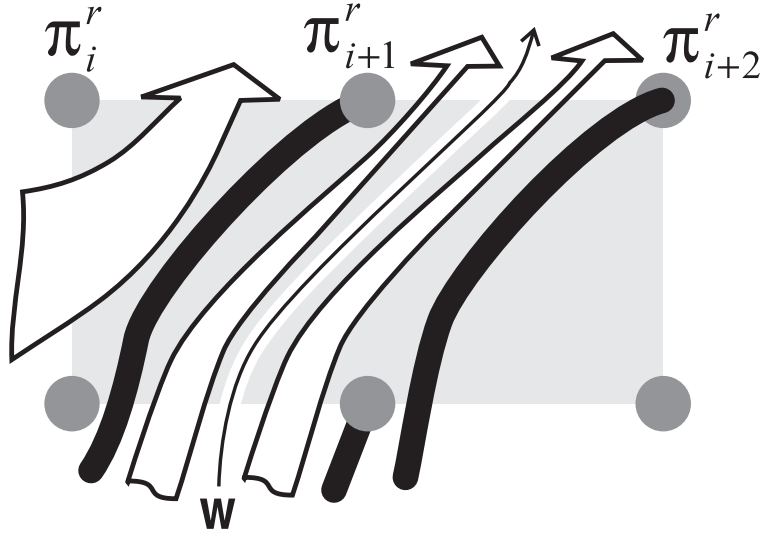
Figure 7: A Wire Intersecting Two Cells Between a Pair of Rings

from the bottom cut. This will not happen because side flow is bounded by $k_r - 1$ according to Lemma 8. Therefore there is no other flow pattern except the three types shown in Figure 6. $\square$

By Lemma 10, the wire that makes the connection in a cell g_i^r always partitions the cell vertically into two disjoint parts. No wire can intersect both left and right side cuts across the cell. This means that a wire cannot enter a cell from one side and leave the cell from the other. Hence any wire can only intersect at most one side cut between two bottom/top cuts. Therefore a wire may intersect two cells between a pair of adjacent rings by intersecting a side cut (Type I Intersection) or it may intersect only one cell between a pair of adjacent rings by not intersecting any side cut (Type II Intersection). $\Gamma(w) \leq 2(r-1)$ where $r = \text{ringof}(w)$. We define $\Gamma_1(w)$ to be the number of Type I intersections, i.e. the number of cells w intersect orthogonally. We define $\Gamma_2(w)$ to be the number of Type II intersections, i.e. the number of cells w intersect diagonally. We have $\Gamma_1(w) + 2\Gamma_2(w) = \Gamma(w)$ and $\Gamma_1(w) + \Gamma_2(w) = r - 1$ where $r = \text{ringof}(w)$. From this result we can state the following:

Lemma 11: *The wire length of a wire w within the pin grid is less than or equal to $\Gamma_1(w) + \sqrt{2}\Gamma_2(w)$.*

Proof: If a wire leaves a cell from the top cut, the length of the wire is equal to the height of the cell which is 1. If a wire w leaves a cell from one of the side cuts, it intersects two cells between

a pair of rings. Figure 7 shows the wire in the cells. Since the ordering of the two cuts B_i^r and T_{i+1}^r is the same, the maximum wire length of w is bounded by the diagonal length which is $\sqrt{2}$ in Euclidean metric. Therefore if the wire intersects $\Gamma_2(w)$ cells diagonally, the bound of wire length is $\sqrt{2}\Gamma_2(w)/2$.

Therefore if the wire w intersects $\Gamma_1(w)$ cells orthogonally and $\Gamma_2(w)$ cells diagonally, the wire length of w is bounded by $Gamma_1(w) + \sqrt{2}\Gamma_2(w)/2$. □

Since the total number of cells a wire intersect does not exceed the number of rings beneath the pin of the wire, $0 < \Gamma_1(w) < r - 1$. From the relation $length(w) = \Gamma_1(w) + \sqrt{2}\Gamma_2(w)$ (Lemma 11) and the relation $\Gamma_1(w) + \Gamma_2(w) = r - 1$, the bounds of a wire can be derived to be $r - 1 < length(w) < \sqrt{2}(r - 1)$.

We can do a better analysis by using the 'Taxicab' wiring metric as discussed by Maley[1]. It is similar to Manhattan wiring metric but the equidistance square is rotated 45 degrees. The distance of a point (x, y) to origin is $(|y + x| + |y - x|)/2$. According to the taxicab wiring metric, the length of a diagonal of a square is the same as the length of a side. Therefore the wire length in diagonally intersected cells is equal to the wire length in orthogonally intersected cells and is equal to 1. Hence *all* wires connected to a given ring has length $length(w) = 1 \cdot \Gamma_1(w) + 1 \cdot \Gamma_2(w)$, which is equal to $r - 1$. This is minimum because the minimum number of cells a wire intersects is also $r - 1$. Hence we have the following theorem.

Theorem 4 (Minimum Wire Length): *EVENPGA produces a topological routing where each wire is of minimum length in taxicab wiring metric.*

6 Implementation and Results

Figure 8 is a 600 pin PGA routed with EVENPGA in the Surf environment. EVENPGA was implemented as a router module of Surf[5]. Surf provides a powerful framework on which the router can be easily built. Specifically, Surf has all the facilities to manipulate rubber-bands as a representation of topological routing. The design-rule enforcement algorithm[7, 9] and geometric transformation algorithm[10, 6] automatically enforces design rules and transforms the topological routing into a detail routing. The run-time of EVENPGA is negligible compared to the generation
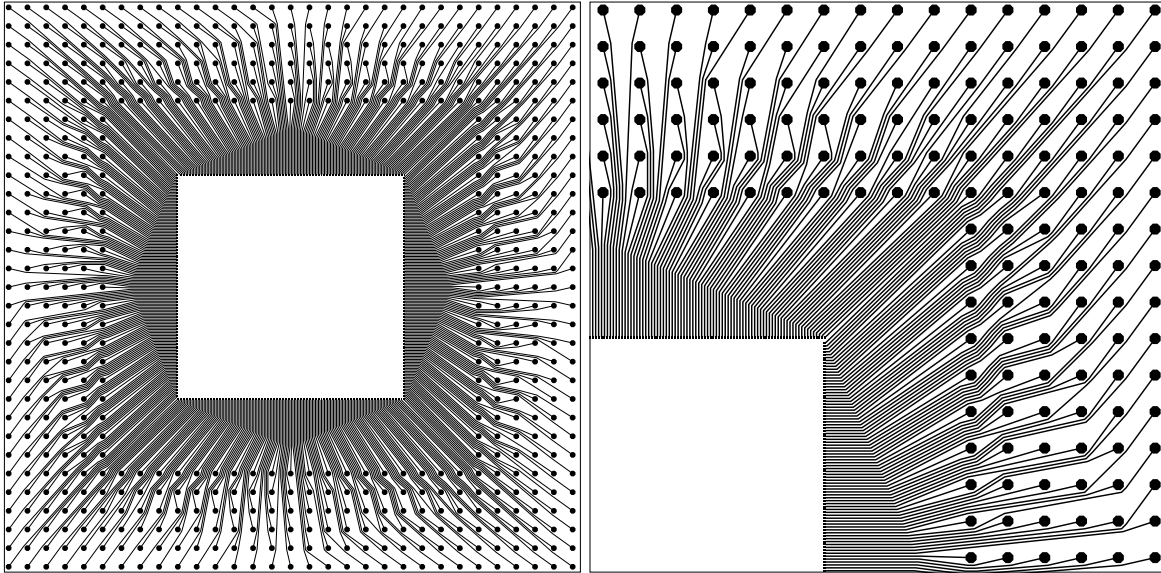
Figure 8: 600 Pin Single-Layer PGA and a Corner

of topological routing (MAKEMTR), and enforcing design rules.

7   Conclusion

This paper studies the pin assignment and routability of a single-layer pin grid array. We have shown that the key to good topological routing is a good pin assignment. This paper is the first to consider both pin assignment and routing and investigated the relationship between the two. We proposed an algorithm that created a good pin assignment that results in a uniformly distributed wires and bounded wire length.

8   Acknowledgment

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