Spectral-Based Multi-Way FPGA Partitioning

Pak K. Chan, Martine D.F. Schlag, and Jason Y. Zien

Computer Engineering
University of California, Santa Cruz
Santa Cruz, California 95064 USA

November 21, 1994

Abstract—Recent research on FPGA partitioning has focused on finding minimum cuts between partitions without regard to the routability of the partitioned subcircuits. In this paper we develop a spectral approach to multi-way partitioning in which the primary goal is to produce routable subcircuits while maximizing FPGA device utilization. To assist the partitioner in assessing the routability of the partitioned subcircuits, we have developed a theory to predict the routability of the partitioned subcircuits prior to partitioning. Advancement over the current work is evidenced by results of experiments on the standard MCNC benchmarks.

I FPGA partitioning

The design flow using commercial FPGA tools involves technology mapping, placement and routing. Since FPGA devices have relatively low density, the use of multiple FPGAs is often required to implement a large circuit. A large circuit has to be decomposed or partitioned into subcircuits for a multiple-FPGA realization, as shown in Fig. 1.

Modifications of standard iterative mincut-based partitioning algorithms have been applied to FPGA partitioning. In [1], Kuznar et al considered the problem of partitioning a circuit for heterogeneous FPGA systems. Their cost function was the total-dollars to implement the circuit. This approach is perhaps suitable from the standpoint of developing a new multiple-FPGA board to realize the given circuit. However, it doesn’t consider the (labor) cost to layout the FPGA systems, where regularity is one of the major design issues. In addition, most existing multiple FPGA systems are homogeneous systems; for example, the Quickturn emulators and reconfigurable FPGA-based computing engines [19, 14]. So there is a need for partitioning algorithms for homogeneous FPGA systems.

Given a large circuit, a partitioner generates many subcircuits. Only when all the subcircuits have been successfully placed and routed, will the multiple FPGAs realize the large circuit. An important issue that has not been considered in the literature is the routability of the partitioned subcircuits. In this paper, we shall see that the manner in which a circuit is partitioned can determine whether all the subcircuits can be automatically routed. We present a theory to predict the routability of partitioned subcircuits prior to partitioning: pre-partitioning routability prediction. The routability predictor can assist a user in determining the number of partitions, and the selection of FPGA devices (when possible) to realize the large circuit.

Knowing the parameters that would affect the routability of the subcircuits, we devise a spectral-based partitioning algorithm to decompose a large circuit into subcircuits. Routability of the partitioned subcircuits is the primary concern. The inputs to our partitioner include partition size and cut constraints. Although spectral-based partitioning algorithms have not been recognized for their ability to realize hard constraints, we shall demonstrate that spectral-based partitioning algorithms are excellent candidates for routability reasons.

In this paper, we shall present two main results on spectral-based partitioning targeted for homogeneous FPGA systems:

1. a theory to predict the routability of the partitioned subcircuits to assist the partitioner in assessing the routability of the partitioned circuits prior to partitioning.
2. a k-way, spectral partitioning method which handles both partition-size and cut-size constraints. The partitioner’s primary goal is to generate routable subcircuits while maximizing logic utilization.

*Supported in part by NSF Grant MIP-9106276 & MIP-9223740 & MICRO Program of University of California

1Supported in part by NSF Grant MIP-9223740 & MICRO Program of University of California.
We compare our partitioning results to those in the literature using the standard MCNC Partitioning 1993 benchmarks. Our partitioner yields partitions which are predictable in the routability sense, while still producing fewer partitions in comparison to results reported in the literature.

II Routability of partitioned subcircuits

A routability barometer has been suggested by the authors in [5] to predict the routability of a single FPGA circuit. We attempt to extend the technique to predict the routability of the partitioned subcircuits. There are two ways to approach this. The straightforward approach is to partition the circuit, and apply the single-FPGA routability predictor to the partitioned subcircuits. We call this post-partitioning routability prediction. A more ambitious approach is to predict the routability of the subcircuits prior to partitioning, and we call this pre-partitioning routability prediction. This approach has the benefit that it can assist a user in determining the number of partitions, and the suitable FPGA devices required to generate routable subcircuits. Given a single FPGA circuit, a single-FPGA routability predictor benefits from the fact that the structure of the circuit can be extracted, hence the average wire length can be estimated with accuracy. Pre-partitioning routability prediction for multiple FPGAs is harder because the structures of the partitioned circuits can only be estimated before partitioning, and the predictions might not be as accurate as the single-FPGA case.

Figure 1 depicts the roles of both routability predictions in the multiple-FPGA design flow. Given a large circuit to be partitioned, the design flow also suggests two possible methods to control the routability of the partitioned subcircuits:

1. remap the given circuit to achieve 100 percent routable subcircuits, and
2. partition the given circuit to facilitate the routability of the subcircuits.

The first method has been the subject of several papers [22, 21, 4]. Here, we shall focus on the second method. Simply put, the routability prediction for a single FPGA circuit involves estimating the channel width requirement of the circuit for routing completion [10]. The parameters of the circuit involved are:

1. \( \gamma \): the average number of pins emanating from each logic block, we shall refer to \( \gamma \) as the pins-per-CLB ratio,
2. \( \beta \): the average number of pins on a net (we refer to \( \beta \) as the pins-per-net ratio), and
3. \( L \): the average wire length of the circuit after placement.

The \textit{average} channel width requirement for routing completion is [10, 5]:

\[
W = \frac{1}{2} \left[ \gamma \cdot \left( 1 + \frac{\beta - 2}{\beta} \right) L \right].
\]
Routability is determined by comparing $W$ with the FPGA device’s channel width. We present a theory to predict the average channel width requirement of subcircuits before partitioning by predicting the average pins-per-CLB and pins-per-net ratios of the partitioned subcircuits (before the circuit is partitioned). The inputs to the routability predictor are:

1. the total number of CLB pins of the (original) circuit,
2. the total number of nets of the circuit,
3. the average wire lengths of the subcircuits,
4. the number of partitions $k$, and
5. the average number of Input/Output pins per partition.

The first two parameters can be calculated from the (unpartitioned) circuit. The average wire lengths of the subcircuits can only be estimated (see Equation (9) later). The last two parameters depend on the devices of the homogeneous FPGA system. Assuming that the pins-per-CLB ratios do not vary widely among the partitioned subcircuits, on the average the pins-per-CLB ratio of a partitioned subcircuit is:

$$\overline{\gamma}_p \approx \gamma = \frac{\text{total CLB pins}}{\text{total CLBs}}.$$  \hspace{1cm} (2)

Similarly, the average pins-per-net ratio of the partitioned subcircuits is

$$\overline{\beta}_p = \frac{\text{CLB and IO pins in a partition}}{\text{nets in a partition}}.$$  \hspace{1cm} (3)

The average pins-per-net ratio $\overline{\beta}_p$ can be estimated with good accuracy, as we shall see. Let

1. $\text{pins}$ denote total CLB pins before partitioning,
2. $\text{pins}_p$ denote CLB pins in partition $p$,
3. $\text{nets}$ denote total nets before partitioning,
4. $\text{nets}_p$ denote (uncut) nets (with one or more pins) contained in partition $p$,
5. $\text{IO}_t$ denote total IOs before partitioning, this is the sum of all IO pins in the original circuit,
6. $\text{IO}_a$ denote total IOs after partitioning, this is the total number of IO pins in all the partitioned subcircuits, and
7. $\text{IO}_b$ denote the number of IO pins in partition $p$.

The number of nets before partitioning and after partitioning can be related as:

$$\text{nets} = \sum_{p=1}^{k} \text{nets}_p - (\text{IO}_a - \text{IO}_b) + \text{nets}_\text{cut by partitioner}$$  \hspace{1cm} (4)

which essentially states that “nets” are conserved. Equation (4) follows from the observation that when a net is partitioned into $t$ pieces exactly $t$ new I/Os will be introduced if the net had no I/O pin to begin with, while only $t-1$ new I/Os will be introduced if it had an I/O pin (if it was already cut). The “$\text{nets}_\text{cut by partitioner}$” term only counts the nets cut by the partitioner which were not connected to the original I/Os. Equation (4) is exact, and on the average:

$$\overline{\text{nets}}_p = \left(\text{nets} + (\text{IO}_a - \text{IO}_b) - \text{nets}_\text{cut by partitioner}\right)/k$$  \hspace{1cm} (5)

so the average pins-per-net ratio is

$$\overline{\beta}_p \approx \frac{\text{average number of pins in a partition}}{\text{average number of nets in a partition}}$$  \hspace{1cm} (6)

$$= \frac{(\text{pins}_p + \text{IO}_p)/\text{nets}_p}{k \cdot (\text{pins}_p + \text{IO}_p)/(\text{nets} + (\text{IO}_a - \text{IO}_b) - \text{nets}_\text{cut by partitioner})}$$

$$= \frac{(\text{pins} + k \cdot \text{IO}_p)/(\text{nets} + (\text{IO}_a - \text{IO}_b) - \text{nets}_\text{cut by partitioner})}{\text{nets}_\text{cut by partitioner} \approx (\text{IO}_a - \text{IO}_b)/\min(k, \beta)}$$  \hspace{1cm} (7)
Figure 2: Tradeoffs between routability and number of FPGAs used to implement the partitioned subcircuits.

since these are the nets that are not connected to the IOs. On the average these nets fanout to $k$ or $\beta$ chips, which ever is smaller. Also, $IO_o = k \times \overline{Io}_p$. So from Equations (6) and (7), we deduce

$$\overline{\beta}_p \approx \frac{(pins + k \times \overline{Io}_p)}{nets + (k \times \overline{Io}_p - IO_k)(1 - 1/min(k, \beta))} \quad (8)$$

Given a circuit, we can extract the number of pins, the number of nets, and the number IO pins, so we know $\beta$. If we know the number of partitions and the average number of IO pins used after partitioning, we should be able to predict the average pins-per-net ratio $\overline{\beta}_p$ prior to the actual partitioning. A good guess of $\overline{Io}_p$ is the number of I/O pins available on the FPGA device. From Equations (1), (2), and (8), we can predict the routability of the partitioned circuits even before partitioning if the average wire length can be estimated. Our approach is to calculate $L$ based on the logic utilization of the FPGA devices and the FPGA device used:

$$L = \sqrt{\text{logic utilization}} \times L_{device, type} \quad (9)$$

where $L_{device, type}$ depends solely on the FPGA device type used. We shall validate our routability theory and Equation (8) through experiments presented in Section IV.

Equation (8) identifies an important aspect of partitioning for routability: the number of IOs $\overline{Io}_p$ has some bearing on the pins-per-net ratio (hence the routability) of the partitioned subcircuits. Equation (8) indicates that $\overline{\beta}_p$ decreases with increasing $\overline{Io}_p$, this suggests that a routability-driven partitioner should maximize the IO utilization, whenever it is possible. Intuitively, a partitioner decomposes the nets of a circuit into inter-partition net and intra-partition nets. Equation (4) expresses the law of “conservation of nets.” Large cut-sizes imply smaller fanout inside the FPGA devices, making the subcircuits more routable.

Figure 2 illustrates the difficult task of a routability-driven partitioner. There are tradeoffs between routability and the cost of devices to implement the partitioned subcircuits. Routability generally increases with reduced utilization, whereas cost decreases with utilization. The art of routability-driven partitioning is to seek the fine balance between routability and cost. It is not obvious that mincut-based algorithms can handle this seemingly paradoxical set of constraints. Typically, mincut-based partitioning algorithms minimize inter-partition cuts [23]. We have devised a spectral-based partitioner that maximizes the IO utilization while minimizing the number of FPGA devices. The partitioner will be discussed in the next section.

III Spectral k-way partitioning

We provide some background to understand spectral-based partitioning. We shall also discuss the subtlety involved in choosing the proper graph matrix (Laplacian or the adjacency matrix) in order to handle both partition-size and cut-size constraints.

III-A Formulation

An instance of the graph partitioning problem consists of a graph, $G = (\mathcal{V}, \mathcal{E})$ with vertices, $\mathcal{V} = \{\nu_1, \nu_2, \ldots, \nu_n\}$, and weighted edges where the weight of edge $e = (\nu_i, \nu_j)$ represents the cost of putting $\nu_i$ and $\nu_j$ in separate partitions. The problem is to find a partition of the set of vertices $\mathcal{P} = \{P_1, P_2, P_3, \ldots, P_k\}$ for a given $k$, which
optimizes some cost criterion based on the weights of the edges cut and/or the sizes of the partitions. The partitioning results can be represented by an $n \times k$ ratioed assignment matrix $R = [r_{ih}]$ where

$$
    r_{ih} = \begin{cases} 
    \frac{1}{\sqrt{|P_h|}} & \text{if } \nu_i \in P_h \\
    0 & \text{if } \nu_i \notin P_h 
    \end{cases} \tag{10}
$$

The rows do not necessarily sum to 1, and column $h$ sums to $\sqrt{|P_h|}$. The related $n \times n$ ratioed partition matrix $P_R = [r_{pij}]$ is defined by

$$
    r_{pij} = \begin{cases} 
    \frac{1}{|P_h|} & \text{if } \nu_i \text{ and } \nu_j \text{ both belong to } P_g \\
    0 & \text{otherwise}
    \end{cases}
$$

For a given partition $P = \{P_1, P_2, \ldots P_k\}$ we have that $P_R = RR^T$.

The adjacency matrix of $G$ is the $n \times n$ matrix $A(G) = [a_{ij}]$ where $a_{ij}$ is the weight of the edge between nodes $\nu_i$ and $\nu_j$. The degree matrix of $G$ is the $n \times n$ matrix $D(G) = [d_{ij}]$ defined by,

$$
    d_{ij} = \begin{cases} 
    \sum_{k=1}^{n} a_{ik} & \text{if } i = j \\
    0 & \text{if } i \neq j
    \end{cases}
$$

The Laplacian of $G$ is the $n \times n$ symmetric matrix $Q(G) = D(G) - A(G)$.

Spectral-based partitioning methods extract global information about the structure of a graph from the eigenvalues/eigenvectors of graph matrices. The relation between the properties of a graph and its spectrum (the eigenvalues/eigenvectors of its associated matrices) has been an area of active research for several years [13, 8, 16, 20]. The spectra of the adjacency matrix $A$ or the Laplacian $Q$ of a graph are the basis for both partitioning [3, 9, 12] and placement techniques [11].

### III-B Spectral ratio-cut partitioning using the Laplacian $Q$

Spectral partitioning forms clusters of vertices based on the embedding implied by the eigenvectors $V$ of a graph matrix, which can be the Laplacian, $Q$, or the adjacency matrix $A$ of the graph.

To minimize the ratio-cut cost metric, researchers used the Laplacian $Q$ to obtain an embedding [18, 2] of the eigenvectors. This is the correct approach since spectral embedding of the Laplacian appears to be closely related to the ratio-cut cost metric.

Let $\Pi$ be the set of all $k$-way partitions of a graph $G$, and $E_h$ be the total weight of the edges in $G$ having exactly one endpoint in partition $P_h$. In [6] the authors show that,

$$
    \min_{X^TX = I} \text{trace}(X^TQX) \leq \min_{P \in \Pi} \sum_{h=1}^{k} \frac{E_h}{|P_h|} \tag{11}
$$

which is a lower bound on $k$-way ratio-cut cost metric. The first $k$ eigenvectors $V_k$ of the Laplacian $Q$ satisfy this inequality and the eigenvectors can be used to form the projector, $VV^T$, as an approximation of the ratioed partition matrix $P_R$.

Note that minimization of the ratio-cut cost metric implies that partition size and partition cut constraints are not imposed simultaneously on the partitions. This is a consequence of the definition of the ratio-cut cost metric.

### III-C Spectral partitioning using the adjacency matrix $A$

The adjacency matrix $A(G)$ of a graph $G$ is a less popular choice of the matrix to obtain an embedding. Based on Donath and Hoffman’s result [9], Rendl and Wolkowicz [20] derived an upper bound on the weight of the edges uncut ($E_{uncut}$) by a partition satisfying pre-determined partition sizes. If $m_1 \geq m_2 \geq \ldots \geq m_k$ are the given partition sizes, $M = \text{diag}(m_1, \ldots, m_k)$, and $\lambda_{n-k+1} \leq \lambda_{n-k+2} \leq \ldots \leq \lambda_n$ are the largest $k$ eigenvalues of the adjacency matrix, then

$$
    \frac{1}{2} \sum_{i=n-k+1}^{n} m_i \lambda_i(A) = \max_{X^TX = I} \left\{ \frac{1}{2} \text{trace}(MX^TAX) \right\} \geq E_{uncut} \tag{12}
$$
Figure 3: (a) Partitions induced by the Laplacian $Q$; (b) Partitions induced by the adjacency matrix $A$.

where $m_i$ is the partition size of partition $i$. If all the partitions have the same size, $m_1 = m_2 = \ldots = m_k = m$, then Equation (12) can be simplified to:

$$
\frac{1}{2} \sum_{i=n-k+1}^{n} \lambda_i(A) = \max_{X^T X = t} \left\{ \frac{1}{2} \text{trace}(X^T A X) \right\} \geq \frac{E_{uncut}}{m}
$$

which is an upper bound on the number of edges uncut. The last $k$ eigenvectors $V_k$ of the adjacency matrix $A$ satisfy this inequality and the eigenvectors can be used to form the projector $V_kV_k^T$. It is an approximation of the ratioed partition matrix $P_R$. Consequently the partitions will be equal-sized, roughly speaking.

We shall use a small example to illustrate the differences in partitioning using $A$ and $Q$. Figure 3 shows a circuit with 3 natural “partitions,” which are unbalanced. We want to partition this circuit into three subcircuits. The partitions induced by using the first 3 eigenvectors of the Laplacian $Q$ are shown in Fig. 3(a). It clearly shows 3 unbalanced partitions which reflect the nature of $Q$ to minimize the ratio-cut cost metric. On the other hand, the partitions induced by using the last three eigenvectors of the adjacency matrix $A$ is shown in Fig. 3(b), reflecting the nature of $A$ to find “balanced” partitions. Hence, the adjacency matrix $A$ is a better choice than the Laplacian $Q$ to partition a circuit for a homogeneous FPGA system.

Equation (8) states that the pins-per-net ratio decreases with increasing number of I/O pins used. So, it is meaningful for a partitioner to find suboptimal cuts for routability purposes. First, a spectral-based partitioner has the inherent property that it can generate a wide selection of cuts. It is easy to see why. For example, from Equation (11), if we exclude the first eigenvector $v_1$ from the minimization, then the lower bound will be increased:

$$
\min_{X^T X = t} \text{trace}(X^T Q X) = \sum_{h=2}^{k+1} \lambda_h(Q) \geq \sum_{h=1}^{k} \lambda_h(Q).
$$

This has the implication that more cuts (consequently more I/O pins) would be obtained by using intermediate eigenvectors to induce the partitions (Similar argument holds for the adjacency matrix). Second, some net models used in transforming hypergraphs into graphs are known to produce more cuts than the others, we may use those net models to increase the cuts. As the last resort, we can use a different graph matrix. For example, use the Laplacian in place of the adjacency matrix.

### III-D From Spectral Embeddings to Partitions

Given the logic capacity and I/O capacity constraints, we present a procedure to use the eigenvector embedding of a graph matrix to construct partitions that satisfy the constraints. As in [6], our approach to $k$-way
KPF_Particle(I/O constraint, logic constraint) |
  Remove high-fanout nets in the hypergraph and transform it to a graph
  Find k eigenvectors of this graph, \( V \)
  Associate each row of \( V \) with its vertex in the original hypergraph
  Mark all vertices unallocated
  \( h=0 \);
  Select vertex with largest-magnitude vector as first prototype
  while (there are unallocated vertices) |
   \( h=h+1 \);
   if \( h \neq 1 \) select vertex most orthogonal to previous prototype
   and use as it as the prototype for partition \( h \)
   Build heap based on the ranking function, Eq. (15)
   while partition \( h \) has not reached logic capacity |
    remove largest cost vertex, \( v \), from heap
    assign \( v \) to partition \( h \)
    update cut tally for each net to which \( v \) belongs
    update heap cost for all vertices adjacent to \( v \)
    put \( v \) on Rollback list if I/O capacity is exceeded
    reset Rollback list if I/O capacity is not exceeded
  |
  Remove vertices on Rollback list from \( h \) and mark them unallocated
  \}
  Print partition results

Figure 4: Pseudo-code for spectral KPF partitioning method. Both I/O and logic capacity constraints are provided by the user.

![Figure 5: Ranking heuristic based on Cuts.](image)

partitioning is to “reverse engineer” the partitions from the embeddings implied by the last eigenvectors of \( A, V = [v_n-k+1, \ldots, v_n] \) (or the intermediate eigenvectors \( V = [v_n-k+1-q, \ldots, v_n-q+1] \), for some \( q \leq n \) if so desired).  

Given the eigenvectors, we measure the cosine of the angle between the two row vectors \( i \) and \( j \) of \( V \) (or the column vectors of \( V^T \)). These **directional cosines** provide a measure of the proximity of the vertices relative to each other. This strategy, in effect, identifies all the ‘1’s in the partitioning matrix \( P \) implied by the projector \( VV^T \).

The first step is to determine a vertex of largest magnitude to serve as the **prototype** (seed) for the first partition. The first prototype is selected by magnitude, and the rest are determined by their relative (anti)orthogonality with respect to the existing prototypes.

A vertex is said to be **allocated** if it has been assigned and committed to a partition. After the determination of the prototype, the rest of the unallocated vertices are ranked based on their anti-orthogonality with respect to the prototype. The ranked vertices are sorted in a heap data structure, which is updated as vertices are extracted from the heap.

An additional factor to be considered in the ranking of the vertices is the number of **cuts** incurred by including a vertex in a partition. The ranking function for the vertices is:

\[
\text{rank} = \text{anti-orthogonality wrt prototype} - f \times \text{cuts incurred}
\]

\[ (15) \]

---

We use the first \( k \) eigenvectors of the Laplacian graph matrix, and the last \( k \) eigenvectors of the adjacency matrix. 

---

1We use the first \( k \) eigenvectors of the Laplacian graph matrix, and the last \( k \) eigenvectors of the adjacency matrix.
The logic capacity and I/O constraints are satisfied by using the procedure KPF as outlined in Fig. 4. In essence, the partitions are built one at a time. A prototype is the first entry of a partition. One at a time, vertices are extracted from the heap and tentatively assigned to the current partition. If the I/O capacity is exceeded, then the vertex's ID is entered into a rollback list. The rollback list is reset if the number of I/Os drops within the bound. Upon each extraction of a vertex from the heap, the heap is (incrementally) updated according to the cost function in Equation (15). The extraction is repeated until the logic capacity constraint is exceeded. Rollback commences if there are entries in the rollback list; it rolls back to the last point where the I/O constraint is met. Then all vertices in the feasible partition are marked “allocated.”

IV Experimental results

IV-A KPF k-way partitioning for FPGAs

We implement our k-way partitioning algorithm with both clustering heuristics pcut and pcluster, and the best results of the two heuristics are presented. We refer to our k-way spectral-based partitioning algorithm as KPF.

We ran the graphs derived from the MCNC FPGA partitioning 1993 benchmarks for the Xilinx XC3000 series. The hypergraphs of the benchmarks were transformed into graphs by using Frankle’s clique expansion net model [11], or the star graph net model. Unlike the clique net model, the star graph net model produces a very sparse graph matrix, which accelerates the eigensolver. On the other hand, this hypergraph model generates auxiliary vertices that have to be filtered out from the eigenvector embedding. We have observed that the star graph net model tends to produce more partitions than the clique net model. Unless otherwise stated, the partitioning results reporting are produced by Frankle’s clique net model.

Also, the hypergraphs of the benchmarks were pre-processed to remove high-fanout nets of degree greater than 99. Nets whose degree were greater than 99 were removed in order to reduce storage space and processing time. This step is essential in facilitating the eigensolver (Scott/Parlett implementation of the Lanczos algorithm [17]) to run on a low-end SPARC station with only 32 Mbyte of memory. The high-fanout nets are...
The routability of all the sub circuits are predicted before they are placed and routed, and the accuracy of the pre-partitioning routability predictor is reported in the last column of Table 2. Subcircuits with zero average unrouted nets indicate successful first-time placement and routing completion. Nonzero average unrouted nets are the averages of 10 placement and routing runs.

Table 2: Routability results of the subcircuits produced by the spectral k-way partitioner KFP for homogeneous FPGA systems using the clique hypergraph model. Reporting the predicted and measured (average) pins/net ratios of the benchmark circuits; also reporting are the prediction of the pre-partitioning routability predictor (r=routable, M=Marginal, U=Unroutable). Subcircuits with zero average unrouted nets indicate successful first-time placement and routing completion. Nonzero average unrouted nets are the averages of 10 placement and routing runs.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>pins/clb predicted by eqn (2)</th>
<th>pins/clb actual average</th>
<th>pins/clb predicted by eqn (8)</th>
<th>pins/clb actual average</th>
<th>CLB % util</th>
<th>% util</th>
<th># of partitions</th>
<th># of unrouted nets in subcircuits Average</th>
<th># of unrouted nets in subcircuits Minimum</th>
<th>pre-partitioning prediction</th>
</tr>
</thead>
<tbody>
<tr>
<td>c3540</td>
<td>5.56</td>
<td>3.95</td>
<td>5.58</td>
<td>3.65</td>
<td>66</td>
<td>99</td>
<td>3</td>
<td>0,0,0</td>
<td>0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>c5315</td>
<td>5.59</td>
<td>3.29</td>
<td>5.68</td>
<td>3.15</td>
<td>63</td>
<td>94</td>
<td>4</td>
<td>0,0,0,0</td>
<td>0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>c6288</td>
<td>4.53</td>
<td>2.46</td>
<td>4.53</td>
<td>2.56</td>
<td>93</td>
<td>77</td>
<td>4</td>
<td>0,0,0,0</td>
<td>0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>s5378</td>
<td>3.24</td>
<td>3.13</td>
<td>5.23</td>
<td>3.19</td>
<td>60</td>
<td>72</td>
<td>2</td>
<td>0,4,55</td>
<td>0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>s9234</td>
<td>5.11</td>
<td>3.11</td>
<td>5.05</td>
<td>3.15</td>
<td>71</td>
<td>69</td>
<td>2</td>
<td>0,0,0,0</td>
<td>0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>s13267</td>
<td>4.70</td>
<td>2.68</td>
<td>4.83</td>
<td>2.79</td>
<td>58</td>
<td>98</td>
<td>11</td>
<td>0,0,0,0,0,0</td>
<td>0,0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>s15580</td>
<td>4.87</td>
<td>2.93</td>
<td>4.90</td>
<td>3.07</td>
<td>66</td>
<td>91</td>
<td>4</td>
<td>2,8,0,0,0,0</td>
<td>0,0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>s38584</td>
<td>5.08</td>
<td>3.27</td>
<td>5.15</td>
<td>3.38</td>
<td>81</td>
<td>95</td>
<td>16</td>
<td>0,0,0,0,0,0,0</td>
<td>0,0,0,0,0,0</td>
<td>✓</td>
</tr>
<tr>
<td>aim1</td>
<td>6.45</td>
<td>3.20</td>
<td>6.45</td>
<td>3.18</td>
<td>58</td>
<td>80</td>
<td>2</td>
<td>3,15</td>
<td>1,11</td>
<td>✓</td>
</tr>
<tr>
<td>misex3</td>
<td>6.49</td>
<td>3.36</td>
<td>6.49</td>
<td>3.36</td>
<td>90</td>
<td>89</td>
<td>2</td>
<td>0,0,0,0,0,0</td>
<td>0,0,0,0,0</td>
<td>✓</td>
</tr>
</tbody>
</table>

The results in Table 1 demonstrate that our spectral-based graph partitioner KPF is capable of handling hard constraints and producing good partitions in reasonable time. We used the results from [15, 7] as references. The partitioner of Kuznar et al [15] is targeted for heterogeneous systems, while our partitioner KPF is targeted for homogeneous systems. We only list our homogeneous partitioning results in Table 1. However, our partitioner is also capable of generating very competitive heterogeneous results. For example, in [15] the authors use a monetary cost function, their partitioner generates a device distribution of

\[ \{0, 0, 1, 0, 1\} \]

meaning one XC3042 and one XC3090 FPGA to implement the benchmark circuit s5378 (routability results are not reported in [15]). But without balancing constraints, our partitioner generates a better device distribution

\[ \{1, 0, 0, 0, 1\} \]

meaning one XC3026 and one XC3090 FPGAs to implement the circuit, and the average CLB utilization is 99.6%. Also, our result is less expensive than [15] with a monetary cost function. But the vendor’s placement and routing tool apr [1] cannot complete the routing of this XC3090 subcircuit, the tool reports 50 unrouted nets! This demonstrates that partitioning without consideration for routability could be an exercise of futility.

Even though several parallel processing researchers reported that in terms of cuts, spectral-based partitioning results can be further improved by applying mincut-based partitioning algorithm such as Kernighan and Lin; we do not resort to this post-processing step for routability considerations. The elapsed times (not CPU time) reported in Table 1 do not include the time taken by an awk script to translate the partitioning results generated by KPF into the Xilinx map format.

IV-B Routability and routability prediction results

The routability of all the subcircuits are predicted before they are placed and routed, and the accuracy of the pre-partitioning routability predictor is reported in the last column of Table 2.
Table 3: Partitioning and routability results of subcircuits of benchmark circuit s15850 generated by using different net models and eigenvectors of the graph adjacency matrix.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>net model</th>
<th>number of partitions</th>
<th>eigenvectors</th>
<th># of CLBs in subcircuits</th>
<th># of IOBs in subcircuits</th>
<th>avg. unrouted nets in subcircuits</th>
</tr>
</thead>
<tbody>
<tr>
<td>s15850</td>
<td>clique</td>
<td>last 2</td>
<td>-</td>
<td>300,299,243</td>
<td>144,143,142</td>
<td>10.3,25.0</td>
</tr>
<tr>
<td>s15850</td>
<td>clique</td>
<td>last 3</td>
<td>-</td>
<td>363,231,156,175</td>
<td>144,144,92,122</td>
<td>7.7,6,6,6</td>
</tr>
<tr>
<td>s15850</td>
<td>clique</td>
<td>last 4</td>
<td>294,191,230,127</td>
<td>144,144,144,92</td>
<td>1.4,0,0,0</td>
<td></td>
</tr>
<tr>
<td>s15850</td>
<td>clique</td>
<td>last 2nd to 4th</td>
<td></td>
<td>249,165,197,231</td>
<td>144,144,137,122</td>
<td>0,0,0,0</td>
</tr>
<tr>
<td>s15850</td>
<td>star</td>
<td>last 3</td>
<td>263,193,127,116,203</td>
<td>143,144,134,143,141</td>
<td>0,0,0,0,0</td>
<td></td>
</tr>
</tbody>
</table>

Table 4: Routability results of subcircuits of alu4 and misex3 after 10 placement and routing runs, showing the effect of increased cuts on routability. The FPGA package XC3042PG132 has a maximum of 144 logic blocks (CLBs) and 56 I/O blocks (IOBs), and the XC3020PC84 package has a maximum of 64 CLBs and 64 IOBs.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>package</th>
<th>net model</th>
<th>subcircuit1</th>
<th>subcircuit2</th>
<th>avg. unrouted nets (subcircuit1,subcircuit2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>alu4</td>
<td>3042PG132</td>
<td>clique</td>
<td>73</td>
<td>81</td>
<td>(4.0, 15.0)</td>
</tr>
<tr>
<td>alu4</td>
<td>3042PG132</td>
<td>star</td>
<td>90</td>
<td>96</td>
<td>(6.0, 11.9)</td>
</tr>
<tr>
<td>misex3</td>
<td>3020PC84</td>
<td>clique</td>
<td>58</td>
<td>57</td>
<td>(0.0, 10.6)</td>
</tr>
<tr>
<td>misex3</td>
<td>3020PC84</td>
<td>star</td>
<td>64</td>
<td>64</td>
<td>(0.0, 6.2)</td>
</tr>
</tbody>
</table>

As we see from the second column in Table 2, the pins-to-cell ratios of the MCNC benchmark circuits are relatively low. All subcircuits predicted to be "routable" automatically completed the routing the first time by apr. On the other hand, subcircuits predicted to be "marginal" didn't complete the routing the first time by apr. Ten placement and routing runs were applied to those subcircuits and the average number of unrouted nets are recorded.

The majority of the subcircuits are predicted to be routable and this was later verified, as given in Table 2. Of particular interest is that circuit s15850 with 3 partitions was predicted to be unroutable, so we increased the number of partitions to 4, and the predictor predicts marginal routability. The prediction was verified to be correct, as depicted in the first five entries, last column of Table 3. This table also illustrates that spectral-based partitioners can generate a wide variety of cuts, and hence partitioning results. For instance, one of the 4 subcircuits generated by using the last 4 eigenvectors (of the adjacency matrix) has 7.7 unrouted (average) nets after 10 apr runs, and this subcircuit has higher cell utilization than the others. Instead, by using the 2nd to 4th eigenvectors our partitioner generates slightly more balanced and routable subcircuits, as indicated in the 4th entry of Table 3. Last, the star net model generates 5 very routable subcircuits, but the utilizations of the subcircuits are low.

We also include two hard-to-route circuits, alu4 and misex3 from the MCNC combinational circuit benchmark suite to test our partitioner and routability predictor. Initially, the circuit alu4 uses two XC3042PG132's and circuit misex3 uses two XC3020PC84's to implement the subcircuits, respectively. The routability predictor predicts the subcircuits to be marginally routable, and this was verified, as shown in Table 2.

We repartition both circuits using the star net model, the results are shown in Table 4. The number of cuts (IOBs) produced by using the star net model is higher than the clique net model. The subcircuits are more "routable" with increased IOB usage, as indicated by the drop in the average number of unrouted nets in Table 4.

We also applied the pre-partitioning routability predictor to check to see if the circuit misex3 would be routed using a different package type, say XC3020PQ100, which has 100 CLBs and 80 IOBs. The predictor predicts positive results and this was verified to be the case.

V Conclusion

In this paper, we have presented partitioning results of a spectral-based partitioner targeted for homogeneous FPGA systems. The partitioner handles both partition-size and cut-size constraints. Routability of the partitioned subcircuits is the primary concern. To assist the partitioner in assessing the routability of the partitioned subcircuits, we have developed a theory to predict the routability of the partitioned subcircuits prior to partitioning. We feel that routability prediction is very valuable and should play an important role in the partitioning for multiple-FPGA systems.
References


