undetected by the stuck-at test sets. In the worst case, where none of the channel-to-row or the cell-to-cell WCA is covered, 20% of the total WCA in the circuit is undetected by the stuck-at tests. On average, most of the shorts from the wiring channel to the cell rows will be detected by the stuck-at tests since the shorts are most likely shorts to the power and ground rails that run parallel to the wiring channel at the edge of the cell rows. This leaves about 17% of the WCA undetected by the stuck-at tests.

## Conclusion

Designing circuits to be more easily testable will help increase the quality of shipped integrated circuits. By designing easily testable circuits, we can avoid a great deal of costly simulations using complex fault models and also minimize the use of costly testing techniques.

In this paper, we have shown that physical design for testability will have a greater impact in cell design rather than in channel routing.

Our next step is to characterize the undetectable shorts and derive a set of design guidelines that can aid circuit designers to minimize the occurrence of these undetectable shorts. Much work has already been done in modifying routing channels to yield more testable designs[11], but a great deal of work still needs to be done examining the shorts within the cells.

## Acknowledgments

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## References

[1] B. Chess, A. Freitas, F. Joel Ferguson, and T. Larrabee. Testing CMOS logic gates for realistic shorts. In *Proceedings of the International Test Conference*, in press. IEEE 1994

[2] B. Chess, C. Roth, and T. Larrabee. On evaluating competing bridge fault models for CMOS ICs. In *Proceedings of the VLSI Test Symposium*, pages 446-451. IEEE 1994.

[3] D. B. I. Feltham and W. Maly. Physically realistic fault models for analog CMOS neural networks. *IEEE Journal of Solid-State Circuits*, vol 26 no 9, pages 1223-1229. IEEE September, 1991.

[4] J. Galiay, Y. Crouzet, and M. Vergniault. Physical versus logical fault models in MOS LSI circuits: Impact on their testability. *IEEE Transactions on Computers*, C-29(6):283-287, June 1980.

[5] F. Joel Ferguson. Physical design for testability for bridges in CMOS circuits. In *Proceedings of the VLSI Test Symposium*, pages 290-295. IEEE 1993.

[6] F. Joel Ferguson and Tracy Larrabee. Test Pattern Generation for Realistic Bridge Faults in CMOS ICs. In *Proceedings of the International Test Conference*, pages 492-499. IEEE, 1991.

[7] A. Jee and C. Bazeghi. Carafe user’s manual. Technical report UCSC-CRL-94-20. University of California at Santa Cruz, 1994.

[8] A. Jee and F. Joel Ferguson. Carafe: an inductive fault analysis tool for CMOS VLSI circuits. In *Proceedings of the VLSI Test Symposium*, pages 92-98. IEEE 1993.

[9] Peter C. Maxwell, Robert C. Aitken, Vic Johansen, and Inshen Chiang. The effectiveness of $I_{DDQ}$, functional, and scan tests: How many fault coverages do we need? In *Proceedings of the International Test Conference*, pages 168-177. IEEE, 1992.

[10] E. J. McCluskey and F. Beulow. IC quality and test transparency. In *Proceedings of the International Test Conference*, pages 295-301. IEEE, 1988.

[11] R. McGowen and F. Joel Ferguson. Eliminating undetectable shorts between horizontal wires during channel routing. In *Proceedings of the VLSI Test Symposium*, pages 402-407. IEEE 1994.

[12] S. F. Midkiff and S. W. Bollinger. Classification of bridging faults in CMOS circuits: experimental results and implications for test. In *Proceedings of the VLSI Test Symposium*, pages 112-115. IEEE 1993.

[13] J. P. Shen, W. Maly, and F. J. Ferguson. Inductive Fault Analysis of MOS integrated circuits. *IEEE Design and Test of Computers*, 2(6):13-26, December 1985.315.

[14] Thomas W. Williams and N. C. Brown. Defect Level as a function of fault coverage. *IEEE Transactions on Computers*, C-30(12):987-988, December 1981.

experiments are the percentages of the WCA of the shorts that fall into each of the following four categories: between interconnection wires, between nodes of the same cell, between an interconnection wire and a node internal to a cell, and between the internal nodes of two adjacent cells. We report the WCA in each of the four categories as a percentage of the total WCA for the entire circuit. Carafe was used to extract the total circuit WCA, the WCA of each row of cells, and the WCA of each individual cell. Hemlock was used to extract the WCA of the interconnection wires of the circuits.

Determining the percentage of the WCA in the interconnect wires and the rows is a straightforward summation and division. To compute the amount of WCA of shorts between the interconnection wires and the cell rows, the sum of the channel and the row areas were subtracted from the total circuit WCA, which should leave the amount of WCA between the channels and the rows of the circuit. For the shorts between adjacent cells in the rows, the sum of the WCA of all the cells that make up the rows multiplied by the number of times each cell was present in the rows was subtracted from the total WCA of the row leaving the amount of WCA of the shorts between adjacent cells.

Table 1. Percentage of WCA areas in each category for the ISCAS'85 circuits.

| | Channel | Cells | Channel-Row | Cell-Cell |
|---|---|---|---|---|
| c432 | 35.06% | 50.48% | 3.38% | 11.08% |
| c499 | 34.63% | 54.04% | 3.44% | 7.89% |
| c880 | 41.00% | 44.78% | 3.86% | 10.36% |
| c1355 | 39.07% | 46.81% | 1.52% | 12.60% |
| c1908 | 40.36% | 48.93% | 2.13% | 8.58% |
| c2670 | 52.20% | 35.28% | 3.00% | 9.52% |
| c3540 | 50.67% | 37.23% | 3.07% | 9.03% |
| c5315 | 59.52% | 29.08% | 2.71% | 8.69% |
| c6288 | 38.90% | 45.92% | 2.01% | 13.17% |
| c7552 | 60.37% | 28.96% | 2.95% | 7.72% |
| Average | 51.80% | 36.01% | 2.70% | 9.49% |

Table 1 contains the data for the percentage of WCA falling in each of the four categories. The average WCA for each category over all the circuits is given at the bottom of the table. We can see that roughly 52% if the WCA is in shorts in the wiring channel while 36% is in the shorts in the cells. The percentage of WCA between adjacent cells in the rows is higher than we would expect. Closer examination showed that a large number of feedthrough cells were being used in the circuit designs. Since the feedthrough cells contained only one wire, virtually all of it's critical area was being attributed to adjacent cell short critical areas. To compensate for this, the data was recomputed. This time, any shorts to the feedthrough lines were filtered out of the calculations. The result of this is shown in Table 2.

Table 2. Percentage of WCA without the feedthrough WCA.

| | Channel | Cells | Channel-Row | Cell-Cell |
|---|---|---|---|---|
| c432 | 35.18% | 50.65% | 7.61% | 6.56% |
| c499 | 34.75% | 54.23% | 5.00% | 6.03% |
| c880 | 41.10% | 44.88% | 9.03% | 4.99% |
| c1355 | 39.23% | 47.00% | 7.93% | 5.85% |
| c1908 | 39.98% | 48.48% | 6.07% | 5.47% |
| c2670 | 52.27% | 35.33% | 8.70% | 3.71% |
| c3540 | 50.79% | 37.32% | 8.42% | 3.47% |
| c5315 | 59.57% | 29.11% | 9.42% | 1.90% |
| c6288 | 38.98% | 46.01% | 9.42% | 5.60% |
| c7552 | 60.44% | 28.99% | 7.96% | 2.61% |
| Average | 51.86% | 36.05% | 8.52% | 3.57% |

Since the overall critical area was reduced, the percentage of WCA in the channels and the cells increased slightly. The WCA of the cell to cell shorts was greatly reduced thus raising the percentage of the channel to row WCA to about three times higher than before.

### Defect Coverage of Stuck-At Tests

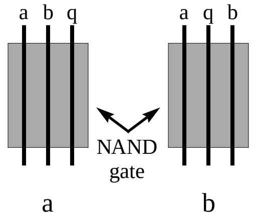
Once the shorts are extracted from the circuit layout, we can simulate them to determine how they affect circuit behavior. Our tool suite can currently simulate and generate tests for shorts that occur in the interconnect wires and shorts that occur within logic cells. In these experiments, stuck-at test sets were used due to the simplicity and wide use of the stuck-at fault model. The test sets were then fault simulated against the interconnect wire shorts and the cell shorts separately. A summary of the results is listed in Table 3. The stuck-at test sets for the ISCAS'85 circuits were generated using the Nemesis test pattern generator run on the netlists extracted by Hemlock.

Table 3. Coverage of stuck-at faults and coverage of the WCA of shorts in the channels and cells.

| | Stuck-At Faults | Channel Short WCA | Cell Short WCA |
|---|---|---|---|
| c432 | 97.16% | 98.00% | 81.73% |
| c499 | 98.98% | 99.87% | 68.64% |
| c880 | 100.00% | 99.31% | 82.72% |
| c1355 | 99.57% | 99.73% | 85.04% |
| c1908 | 99.28% | 98.83% | 74.67% |
| c2670 | 96.29% | 95.65% | 74.68% |
| c3540 | 96.58% | 99.33% | 83.17% |
| c5315 | 98.79% | 99.62% | 83.98% |
| c6288 | 99.42% | 99.73% | 85.03% |
| c7552 | 98.39% | 98.13% | 77.85% |
| Average | 98.59% | 97.85% | 81.05% |

On average, about 98% of the WCA in the channel is covered by the stuck-at tests. This means that about 1% of the total WCA of the circuit is undetected by the stuck-at test and lies in the channel. For the cells, about 81% of the critical area is covered. This means that about 7% of the WCA of the circuit is undetected by the stuck-at tests and lies in the cells. In the best case, where all of the channel-to-row and cell-to-cell WCA are covered, about 8% of the total WCA is that detects an input stuck-at 0 or 1 will detect a short between that input and q, whereas a short between the inputs is undetectable as a logic fault. The intent of the research leading to this paper is to identify possible characteristics in physical design that lead to undetectable faults such as this one.

Fig. 2. Two possible designs for the I/O of a 2-input NAND gate.



## Fault Analysis Tools

To facilitate our research, we have developed a set of tools that extract the list of possible shorts and determine how the shorts affect the circuits' behaviors. This section contains a brief description of these tools.

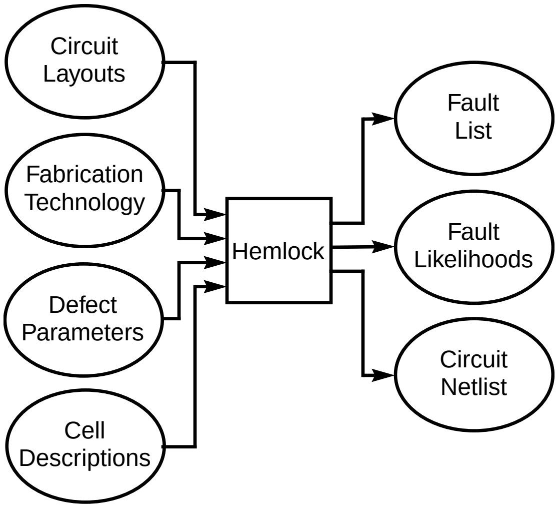
### Fault Extraction Tools

As mentioned in the previous section, the first step in the research is to extract the list of possible shorts that may occur in the circuit layout as a result of defects. The Carafe Inductive Fault Analysis tool was used to extract the faults from the circuit layouts[8]. Carafe takes the layout of a circuit and a description of the defects and extracts the list of possible shorts along with the critical area where a defect may cause the short to occur.

There are occasions where the fault list generated by Carafe may become unwieldy due to its size. Also, Carafe generates fault lists at the transistor level and few fault simulators and test pattern generators can deal with faults at the transistor level. To address both of these problems, we modified Carafe so that it can extract faults only from the interconnect regions (wiring channels) of the circuits using modified layouts. This version of Carafe was developed for use with the Hemlock realistic fault test pattern generation system and is referred to here as just Hemlock[6].

By using circuit layouts that have all the interconnect wiring at the top level hierarchy and the cells at the next lower level of the hierarchy, Hemlock extracts the interconnect faults as well as a gate level netlist for the circuit. To extract the gate level netlist, Hemlock requires a file that describes the locations of the inputs and outputs of the cells in order to correctly connect the interconnection wires with the logic gates. Figure 3 is a diagram of the various inputs and outputs of the Hemlock version of Carafe.

Fig. 3. The inputs and outputs of the Hemlock version of Carafe.



### Fault Behavior Tools

After we have the list of shorts, we must determine their behavior before we can judge whether a short is easily detected or difficult to detect. To do so, several tools have been developed. For the shorts that occur in the interconnect wires of the circuit, the system described in [2] can both determine the behavior of the circuit and generate a test pattern for the faulty behavior using the Nemesis test pattern generator. Similarly, for shorts occurring within a logic cell, a system has been developed to determine the behavior of the cell with a short and to develop test patterns for the cell in a larger circuit based on that faulty behavior[1].

## Experimental Data

In this section, we present our findings on the locations of the defects that may cause shorts to occur. Also presented are weighted critical area coverages of stuck-at test sets.

### Experimental Conditions

In these experiments, we analyzed the set of ISCAS'85 combinational benchmark circuits. Layouts for these circuits were created by MCNC using their technology mapping, placing and routing tools. For these experiments, we have used their layouts scaled to 1.2µ design rules.

The weighted critical area (WCA) is the critical area of a fault weighted by the probability of occurrence of the defect causing the fault. To obtain somewhat realistic WCAs from Carafe and Hemlock, we used defect distributions as reported for a typical digital CMOS fabrication technology[3]. The actual fabrication statistics file for Carafe and Hemlock was generated from that data and the Fabit program[7].

### Locations of the Short Causing Defects

The data that we would like to see from these

# An Analysis of Shorts in CMOS Standard Cell Circuits

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***Abstract* — In order to provide high levels of IC quality, we must be able to detect the presence of a very high percentage of the defects that may occur in circuits. Our long term goal is to address this problem by developing guidelines to design circuits to be more easily tested without requiring complex fault models or testing techniques. This paper is a first step towards this goal. This paper contains data on which shorting defects are most likely to occur in CMOS standard cell circuits and which are most likely to not be detected by standard testing methods.**

## Introduction

To ensure that very few ICs containing defects are delivered to customers, we must be able to detect a very high percentage of the defects that may occur in the ICs[9][10][14]. Unfortunately, many of the defects that may occur in CMOS circuits do not manifest themselves as faults that are detectable by traditional tests[4][13]. Thus, a great deal of research has been done to create more accurate fault models and test methods to detect these defects[1][2][6]. These solutions tend to require time consuming simulations or longer test times to be useful. We are investigating how circuits can be made more easily testable by changing their physical design, not by requiring the addition of any circuitry. By designing circuits to be more testable, it will be easier to detect a high percentage of the possible defects without resorting to complex fault models and test application techniques.

In this paper, we report on the results of our investigations of where short causing defects tend to occur in CMOS standard cell designs. This work is similar to that in [12], but the focus of this work is on the actual defects causing shorts rather than the shorts themselves. We first describe the research that we are working on, followed by a presentation of the fault extraction tools we use. A description of the experiments and the resulting data are presented and the paper closes with a short conclusion.

## Research Goal

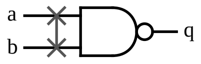
The results presented in this paper will be used in the future to direct our design for testability research. The goal of this research is to develop a set of guidelines that will aid designers in creating circuits that are easily testable for defects that cause shorts. This research concentrates on standard cell design styles.

The first step in this research is to determine where the defects that can cause shorts may occur in the layout of the circuits. To do this, we have developed a set of software tools that can analyze the layouts of circuits in the presence of defects and determine whether a short can occur as a result of the given defect. These tools are discussed in more detail later.

Once the locations of the shorts are extracted (location in the layout and in the netlist), the characteristics and behaviors of the shorts are analyzed by simulating the faulty circuit using the Spice circuit simulator. We then attempt to generate a test for the short and determine if it is detectable. If the short is undetectable, we then examine the physical location of the short and determine what characteristics of the short make it difficult to detect. Similarly, we may find characteristics that make the shorts easy to detect. With this information, we can develop a set of layout design guidelines that can be used to create circuits that are more testable.

One example of a cell level design guideline is for a 2-input NAND gate. Consider the short across its inputs as shown in Figure 1. Circuit simulations have shown that, for most driving cells, the short exhibits wired-AND behavior making the short undetectable by observing the logic values at the output of the gate.

Fig. 1. A 2-input NAND gate with a short across its inputs.



If the inputs and outputs of the NAND gate were designed as in Figure 2a, there is a possibility of a defect causing the difficult-to-detect short to occur. However, if the NAND gate was designed as in Figure 2b, that short cannot occur since a defect large enough to short inputs a and b together would also short to output q. However, a short between either input and q is possible. This usually results in the input value dominating the output value. In effect, any test

# An Analysis of Shorts in CMOS Standard Cell Circuits

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ABSTRACT

In order to provide high levels of IC quality, we must be able to detect the presence of a very high percentage of the defects that may occur in circuits. Our long term goal is to address this problem by developing guidelines to design circuits to be more easily tested without requiring complex fault models or testing techniques. This paper is a first step towards this goal. This paper contains data on which shorting defects are most likely to occur in CMOS standard cell circuits and which are most likely to not be detected by standard testing methods.

**Keywords:** Shorts, Inductive fault analysis, defect, Carafe