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Figure 10: Voltage response of the clock network.

for the analysis. The model provides adequate accuracy for submicron CMOS technology. It takes into account the nonlinear nature of the active devices and yet is efficient enough to use in fast transient interconnect analyses. Computationally, by combining MEF approximation with the new driver model, a two order of magnitude improvement over traditional circuit simulator is demonstrated with comparable accuracy in high speed interconnect transient analysis. The efficiency of the algorithm makes accurate analysis of large systems practical.

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Figure 8: Voltage response of the RC circuit.

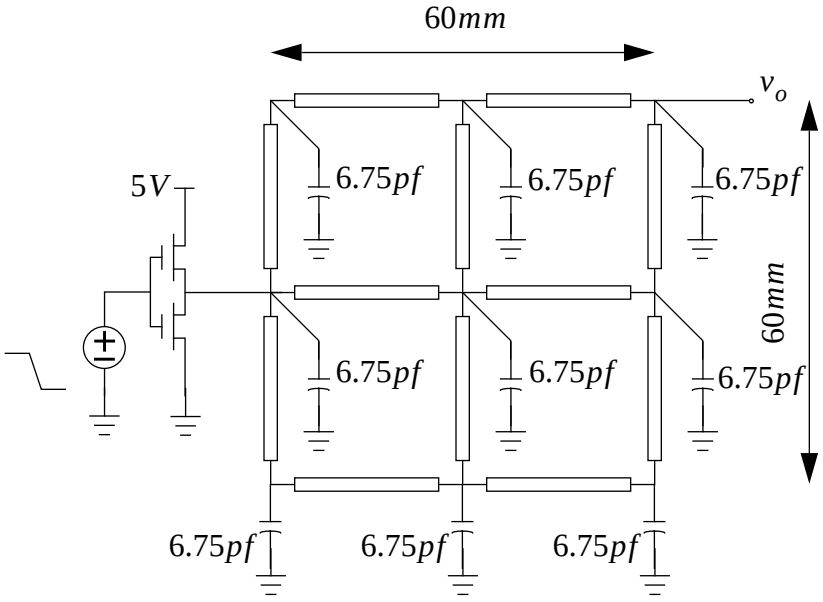

Figure 9: A grid-type clock network.

alyze the circuit on a SUN Sparc 1+ workstation. Our method took only 1.9 seconds CPU times, and most of them is for I/O process. Figure 10 shows the voltage response.

8 Conclusions

We have discussed two important issues related to transient interconnect analyses. Based on a S-parameter macro model, a new approximation function, MEF, is introduced to accurately analyze a system of interconnects with nonlinear drivers. Our method can provide stable solution with any degree of accuracy. We have also presented an improved nonlinear driver model suitable

$$value \leftarrow (value \times t/d - d \times coe)\, e^{-t/d} + d \times coe$$

$$value \leftarrow value \times \text{slope\_of\_ramp}$$

The proof of the algorithm is omitted for brevity. The complexity of the above algorithm is $O(n)$, where n is the order of $h_e(t)$. Convolution of the n^{th} order $h_p(t)$ with the current input is also an $O(n)$ algorithm.

Similarly, convolution of $h_p(t)$ and $h_e(t)$ with a step or exponentially decaying function can be computed with time domain explicit formulas or recursive formulas.

7 . Experimental Results

Two examples are given below. The first circuit is an RC circuit with floating capacitors (See Figure 7). The driver model parameter includes maximum current ($11.2mA$), threshold volt-

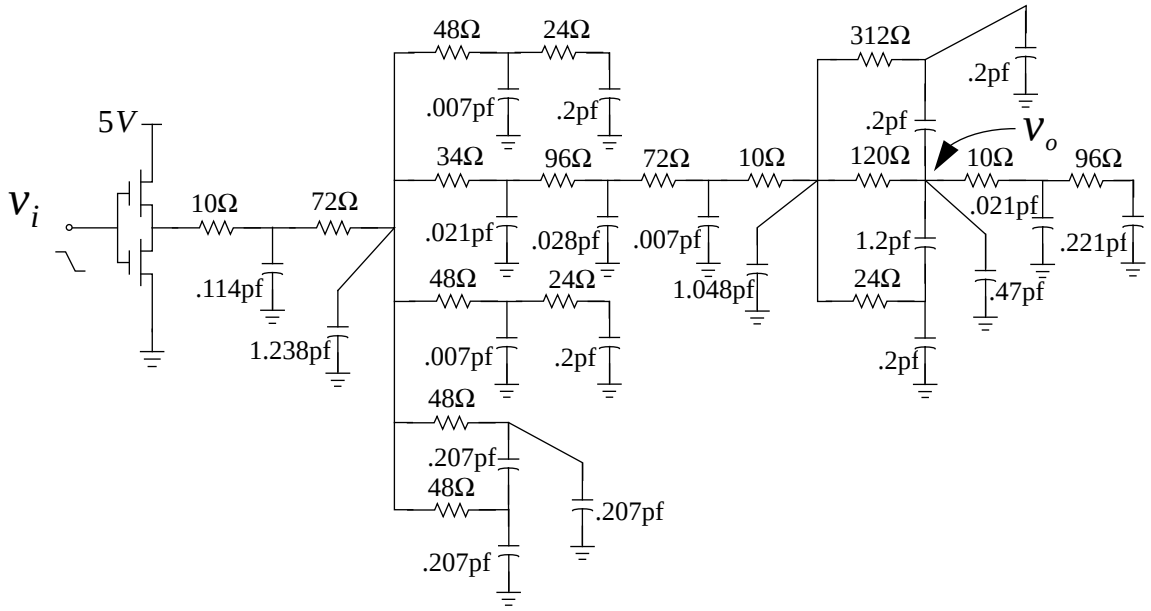

Figure 7: An RC circuit with floating capacitors.

age ($1.0V$) and the rise time of the input signal ($1.0ns$). Output voltage V_o computed by MEF transient analysis method are compared with SPICE result in Figure 8. Throughout our experiments, the SPICE level one MOS transistor models are used for SPICE simulations.

The second example is a grid-type clock network (See figure 9). The clock is distributed around the periphery of a $60mm \times 60mm$ chip. The vertical runs are on metal 1 ($R = 0.06\Omega/mm$, $L = 0.548nH/mm$ and $C = 0.1423pF/mm$) and the horizontal runs are on metal 2 ($R = 0.04\Omega/mm$, $L = 0.5025nH/mm$ and $C = 0.1552pF/mm$). The parameters of the driver are: maximum current $28.8mA$, threshold voltage $1.0V$ and the rise time of the input signal is $1.0ns$. With direct convolution, SPICE3e2 took more than 200 seconds CPU times to an-

approximation for a wide range of CMOS gates. Next section focus on how to combine this driver model with MEF approximation of the interconnect for transient analysis.

6 . Response Function

Combined with the load, the current flowing into the interconnects driving by the current model can be piecewisely expressed. For $t_{linear} \geq t_r$, the current is [6]

$$\begin{aligned} i(t) \;=\; & w\,(t - t'_{th})\,u(t - t'_{th}) - w\,(t - t_r)\,u(t - t_r) \\ & - I_{max}u(t - t_{linear}) + I_{max}e^{-(t - t_{linear})/\tau}u(t - t_{linear}) \end{aligned} \tag{30}$$

where w is the slope of the current wave in rising ramp section (See Figure 4(c)). Similarly, for $t_{linear} < t_r$, the output current of the current model also can be expressed piecewisely. In other words, the current is the overlay of step, ramp and exponentially decaying functions. The transfer functions of the interconnects including the driving point impedance can be approximated by MEF, $h(t) \;=\; h_p(t) + h_e(t)$. $h_p(t)$ is the sum of exponentials (See Eq. 10), and $h_e(t)$ is the exponentially decayed polynomial function (See Eq. 14). The output response $V_o(t)$ is

$$V_o(t) \;=\; h(t) * i(t) \;=\; h_p(t) * i(t) + h_e(t) * i(t) \tag{31}$$

where * represents convolution. To symbolically convolve $h_p(t)$ with the input we take the convolution of each term in $i(t)$ with each term in $h_p(t)$. The effect of the rising ramp on an exponential can be explicitly represented by:

$$wt * (k_i e^{p_i t}) \;=\; \begin{cases} \dfrac{1}{2} w k_i t^2 & p_i \;=\; 0 \\ \dfrac{w k_i}{p_i^2}\,(e^{p_i t} - p_i t - 1) & p_i \neq 0 \end{cases} \tag{32}$$

The convolution of $h_e(t)$ with input can be computed by recursive formulas. For example, the effect of the rising ramp on the n^{th} exponentially decayed polynomial function is

$$F_n(t) \;=\; wt * h_e(t) \;=\; w \sum_{j=0}^{n} t * (c_j\,(\frac{t}{d})^j e^{-t/d}) \;=\; w \sum_{j=0}^{n} c_j\,(t f_j(t) - d f_{j+1}(t)) \tag{33}$$

with $f_{j+1}(t) \;=\; (j+1)\,f_j(t) - d\,(t/d)^{j+1} e^{-t/d}$ and $f_0(t) \;=\; d\,(1 - e^{-t/d})$. Based on the Eq. (33), we have a simple algorithm to implement the convolution process:

$value \leftarrow 0,\ coe \leftarrow 0$

for $(j \leftarrow \text{order};\ j \geq 0;\ j \leftarrow j - 1)$

$coe \leftarrow coe - c_j \times d$

$value \leftarrow value \times t/d - d \times coe$

$coe \leftarrow c_j \times t + (j+1) \times coe$

used to determine if there is a grounded resistive element.

Theorem 1: An interconnect system has no grounded resistive element if and only if the driving point s-parameter is equal to one at frequency $s = 0$, that is, the first moment of S_{in} is equal to one.

Proof: Consider the relation between the scattering parameter and the impedance, we have

$$S_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{24}$$

where Z_0 is the reference impedance. If there is no grounded resistive elements, the driving point impedance $Z_{in} = \infty$ at $s = 0$, thus $S_{in}(0) = 1$. On the other hand, rewrite the above equation

$$Z_{in} = \frac{1 + S_{in}}{1 - S_{in}} Z_0 \tag{25}$$

If $S_{in}(0) = 1$, then $Z_{in}(0) = \infty$, indicates no grounded resistive elements.

From the property of Taylor series, the second moment of the $S_{in}(s)$ is $\frac{d}{ds}S_{in}(0)$. The following theorem shows that the equivalent driving point capacitance is only dependent on the second moment of S_{in}.

Theorem 2: For an interconnect system with no grounded resistive element, the equivalent driving point capacitance is

$$C_{eqv} = -\frac{1}{2Z_0}\frac{d}{ds}S_{in}(0) \tag{26}$$

Proof: From Eq. (25), since $S_{in}(0) = 1$, there is a pole at $s = 0$ for driving point impedance. The corresponding residue is

$$k_0 = \left.\frac{(1 + S_{in})\, Z_0}{\frac{d}{ds}(1 - S_{in})}\right|_{s=0} = -\frac{(1 + S_{in}(0))\, Z_0}{\frac{d}{ds}S_{in}(0)} = -\frac{2Z_0}{\frac{d}{ds}S_{in}(0)} \tag{27}$$

and the equivalent driving point capacitance is

$$C_{eqv} = \frac{1}{k_0} = -\frac{1}{2Z_0}\frac{d}{ds}S_{in}(0) \tag{28}$$

Consequently, the pole at $s = 0$ makes it impossible to express the driving point impedance in Taylor series. In this case, the function to be matched with a mixed exponential function becomes

$$Z'_{in} = Z_{in} - \frac{1}{C_{eqv}s} \tag{29}$$

We have thus completed the construction of the driver model. This new model is an accurate

The computation is based on the following equation [8]:

$$v_{in}(t_{linear}) + |V_{th}| = v_{out}(t_{linear}) \tag{18}$$

In this case, the initial current value in section 4 is

$$i_0 = \frac{t_{linear} - t'_{th}}{t_r - t'_{th}} I_{max} \tag{19}$$

Note that in this case, t_{linear} is less than t_r.

Next, we consider the computation of the time constant τ used in section 4 of the model. It is desirable to be able to compute the time constant without adjusting the process proposed in [6]. Since the initial current of section 4 is known, the exponential decay function is determined solely by its time constant. Assume that output current in this section is

$$i_{out}(t) = i_0 e^{-(t - t_{linear})/\tau} \tag{20}$$

So, the charge pumped into section 4 is $i_0\tau$. The total charge in section 1, 2 and 3 are

$$Q_{prev} = \begin{cases} ((t_r - t'_{th})/2 + t_l - t_r) I_{max} & (t_l \geq t_r) \\ (t_l - t'_{th})^2 I_{max}/2\,(t_r - t'_{th}) & (t_l < t_r) \end{cases} \tag{21}$$

Thus, we can determine the time constant τ by

$$i_0\tau + Q_{prev} = C_{eqv} V_{DD} \tag{22}$$

where C_{eqv} is the equivalent driving point capacitance. In the next section, we will describe how to compute the equivalent driving point capacitance from the scattering parameter based macromodel. Once the capacitance is found, time constant τ can be directly determined by Eq. (22).

5 . Computation of the Equivalent Driving Point Capacitance

For the s-parameter interconnect macromodel described earlier in this paper, we can easily find the driving point s-parameter and then get the equivalent capacitance. Without loss of generality, assume a two port network (See Figure 6) is the result of the network reduction process. The

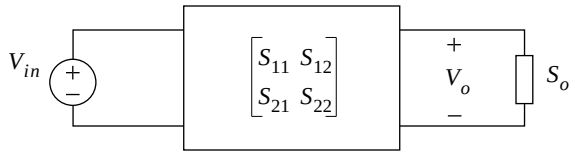

Figure 6: A two port network.

driving point s-parameter in frequency domain is

$$S_{in} = S_{11} + \frac{S_{12}S_{21}S_o}{1 - S_{22}S_o} \tag{23}$$

Before we proceed to compute the equivalent capacitance, the following theorem can be

Figure 5: Driver model currents vs. actual current

this current model is even more significant. In order to compensate the nonlinear current, we introduce a virtual threshold point t'_{th} for the linear current source model (See Figure 4 (d)). The modified driver model does not start to conduct current until time t'_{th}. Note that the slope at which the current changes is also affected by t'_{th}. Let charge pumped into the interconnect by current model described by Eq. (15) be equal to the charge pumped by our linearly increasing current model, we have

$$t'_{th} = \frac{2}{3}t_{th} + \frac{1}{3}t_r \tag{16}$$

Where t_{th} is the time at which the input voltage satisfies the following condition:

$$V_{DD} - v_{in}(t_{th}) = |V_{th}| \tag{17}$$

Shown with dotted line in Figure 5 is the new current source model. As one can easily see, this new current model approximates the actual current of the nonlinear driver with much improved accuracy.

If the equivalent driving point capacitance is large enough, the section 2 model is employed until the time t_r at which the input transition reaches its final value, then switches to section 3. If the equivalent driving point capacitance is small, PMOS turns on in the linear region, the gate thus enters section 4 directly. The method to determine which case will occur is by computing output voltage v_{out} at the time t_r with the assumption that the load is driven by this linearly increasing current model. If $v_{out}(t_r) < |V_{th}|$, PMOS is still in the saturation region, the gate operates in section 3; otherwise, we need to compute t_{linear}, at which the PMOS turns on in the linear region.

governing MOS transistors. It takes into account the nonlinear effect of the driving gates and yet it is simple enough for fast transient analyses. By lumping the input and output capacitors of the active gates into the interconnect networks, the amplitude of the current flowing out of the gate at any instant is the function of input and output voltages of the driver at that instant. Consider a CMOS inverter. For a falling input voltage transition shown in Figure 4(b), the corresponding output current is piece-wisely modeled in four sections[6].

As illustrated in Figure 4(c), the output current of the driver in Section 1 is equal to zero since the source to gate voltage of the PMOS transistor is less than its threshold voltage and the source-drain voltage of the NMOS transistor is zero. As the input voltage decreases, the source to gate voltage of the PMOS transistor exceeds its threshold voltage, causing it to turn on in saturation. The NMOS transistor starts from the linear region, enters saturation and finally, into cutoff region. This section is modeled by a linearly increasing current source with slope $I_{max}/(t_r - t_{th})$, where t_{th} is the time when the PMOS transistor starts conducting current and I_{max} is the maximum current the gate provides. Section 3 begins at t_r, when the PMOS transistor is in the saturation region and NMOS in the cutoff region. A constant current source with amplitude I_{max} represent the model. When the output voltage rises to a value such that PMOS transistor enters its linear region, section 4 of the model takes effect. In the linear region, the transistor with the constant input voltage behaves like a linear resistor. The output current is modeled by an exponential decay function as the output voltage reaches its final value. The time constant τ is initially computed based on the charge which has been pumped into the loading network. This initial guess of τ needs to be scaled so that the final voltage at the output of the gate is correct. It is assumed that there are no grounded resistive elements in the system.

Here, we present two major improvements to the above driver model. Let's first discuss section 2 in detail. In this section, PMOS transistor current increases quadratically, while the NMOS transistor current increases linearly for a while, then quadratically decreases to zero. Ignoring the small current of the NMOS transistor, the current flowing into the interconnect should be

$$i_0 = \frac{I_{max}}{(t_r - t_{th})^2}(t - t_{th})^2 \tag{15}$$

Using a linear current source as shown in Figure 4 (c) to approximate this quadratic current will result in a large error, especially for a slow rising/falling input signal. The broken line in Figure 5 shows the comparison of current given by this current model and the actual current flowing out of the gate obtained by SPICE simulation. As one can see, the linear current begins to increase much earlier than the actual current, more charges are pumped into the load at the beginning of the transition causing the PMOS transistor to fall out of the saturation region before the current reaches its real final value. When the NMOS transistor current is not negligible, the inaccuracy of

4 . Driver Model

To obtain the transient response of a system of nonlinear elements connected by linear interconnects, the time domain transfer function of the interconnect, *h(t)*, derived in the last section, needs to be combined with proper driver models. The traditional simple Thevenin equivalent circuit is not adequate to describe a submicron nonlinear gate. This section is therefore, aimed to find an accurate yet efficient model for the nonlinear gates.

A current source model is proposed in [6] to model the current output waveform of nonlinear CMOS drivers (See Figure 4(a)). The model is based upon the first order analytical model

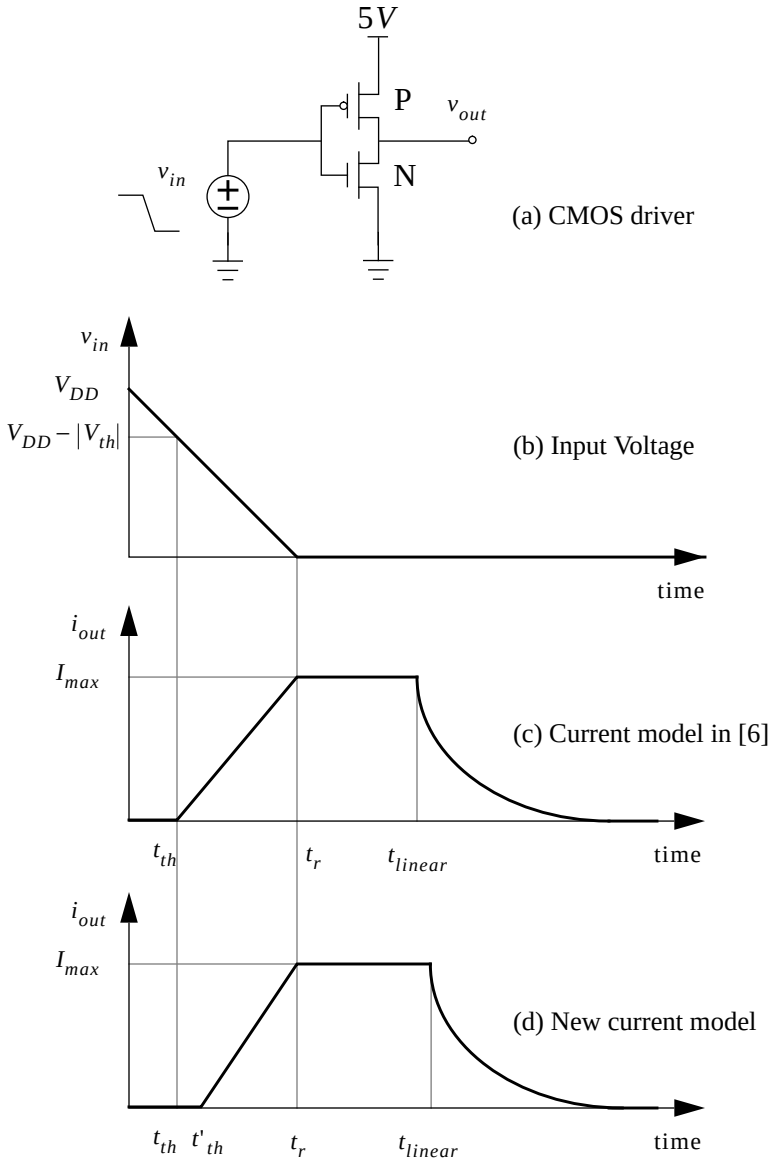

Figure 4: Input voltage transition and the current source model.

While EDPF gives a stable approximation, it is found that to obtain the same degree of accuracy, a higher order EDPF function is required compare to Pade approximation when stable solution can be found for the later. Hence, it is of computational advantage to choose Pade approximation over EDPF when possible. Comparing the characteristics of Pade approximation and EDPF, we propose a Mixed Exponential Function (MEF) approximation for the analysis of interconnect networks. MEF is the combination of the exponential function and exponentially decayed polynomial function.

We use MEF to approximate the transfer function with $2q$ moments shown in Eq. (7) in two steps. First, a qth order exponential function $h_p(t)$ is used to match Eq. (7) in time domain with Pade technique. Clearly, $h_p(t)$ completely matches all $2q$ moments of the transfer function $H(s)$. If all poles of $h_p(t)$ are stable, the process of time domain synthesis of the transfer function is completed.

If there exist unstable poles, the corresponding terms in $h_p(t)$ are discarded. Let there be q_p $(q_p < q)$ stable poles, then $h_p(t)$ becomes

$$h_p(t) = \sum_{i=1}^{q_p} k_i e^{p_i t} \tag{10}$$

Transfer $h_p(t)$ into frequency domain and expand it around $s = 0$, we have

$$H_p(s) = \sum_{i=0}^{2q-1} m_{pi} s^i \tag{11}$$

where m_{pi} is the ith moment of $H_p(s)$, and

$$m_{pi} = -\sum_{j=1}^{q_p} k_j p_j^{-i-1} \tag{12}$$

Since unstable poles in $h_p(t)$ are not included, $H_p(s) \neq H(s)$. Let

$$H_e(s) = H(s) - H_p(s) = \sum_{i=0}^{2q-1} m_{ei} s^i \tag{13}$$

where $m_{ei} = m_i - m_{pi}$. A q_e^{th} $(q_p + q_e \geq q)$ order EDPF function is then used to match $H_e(s)$ [3]. In the time domain, we have:

$$h_e(t) = \sum_{i=0}^{q_e} c_i \left(\frac{t}{d}\right)^i e^{-(t/d)} \tag{14}$$

Finally, $h(t) = h_p(t) + h_e(t)$ is the time domain synthesis of transfer function $H(s)$.

As pointed out earlier, MEF preserves the high accuracy of Pade approximation with guaranteed stable solution.

troduced. Let

$$A = \sum_{i=0}^{n} a_i s^i, \qquad B = \sum_{i=0}^{n} b_i s^i \tag{4}$$

Then, a *Multiplication Operation* is defined as:

$$C = A \times B = \sum_{i=0}^{n} c_i s^i \qquad with \qquad c_i = \sum_{j=0}^{i} a_j b_{i-j} \tag{5}$$

And a *Division Operation*:

$$D = A/B = \sum_{i=0}^{n} d_i s^i \qquad with \qquad d_i = \frac{1}{b_0}\left(a_i - \sum_{j=0}^{i-1} d_j b_{i-j}\right) \tag{6}$$

The s-parameters of all elements can be expanded into Taylor series. Thus, based on the adjoined merging and self merging rules with series operations, the s-parameters of the final multiport is derived in Taylor series. The various transfer function can be obtained from the s-parameters of the macromodel.

3 . Time Domain Description of Macromodel with a Mixed Exponential Function

A frequency domain transfer function with $2q$ moments,

$$H(s) = \sum_{i=0}^{2q-1} m_i s^i \tag{7}$$

can be approximated with the following summation of time domain exponential functions using the n^{th} order Pade approximation [5]:

$$h_p(t) = \sum_{i=1}^{n} k_i e^{p_i t} \tag{8}$$

Where p_i and k_i are the poles and residues, respectively. The Pade approximation provides a relatively accurate and efficient way to evaluate the response of linear interconnect systems. However, it suffers from the stability problem: unstable poles may be generated for known stable networks. That is, p_i may lie in the right half complex plane.

In order to overcome this problem, Exponentially Decayed Polynomial Functions (EDPF)[1, 3] are used to approximate the transfer function of the macromodel. EDPF can approximate the time domain transfer function with any degree of accuracy. And its corresponding frequency domain function has only one repeated stable pole, so it is always stable for stable systems. An n^{th} order EDPF in time domain has the following form:

$$h_e(t) = (c_0 + c_1\frac{t}{d} + c_1(\frac{t}{d})^2 + \ldots + c_n(\frac{t}{d})^n)\, e^{-(t/d)} \tag{9}$$

where d is the time constant.

and *Y*, the resultant $(n+m-2)$ port system has the following s-parameters:

$$S_{ji} = \begin{cases} S_{ji}^{(X)} + \dfrac{S_{ki}^{(X)} S_{ll}^{(Y)} S_{jk}^{(X)}}{1 - S_{kk}^{(X)} S_{ll}^{(Y)}} & i, j \in X \\ \dfrac{S_{ki}^{(X)} S_{jl}^{(Y)}}{1 - S_{kk}^{(X)} S_{ll}^{(Y)}} & i \in X, j \in Y \end{cases} \tag{1}$$

Self Merging Rule: Let *X* be an *m* port system with a self loop connected to the l^{th} and k^{th} ports in X, as shown in Figure 3. After eliminating the self loop, the resultant (*m* - 2) port system

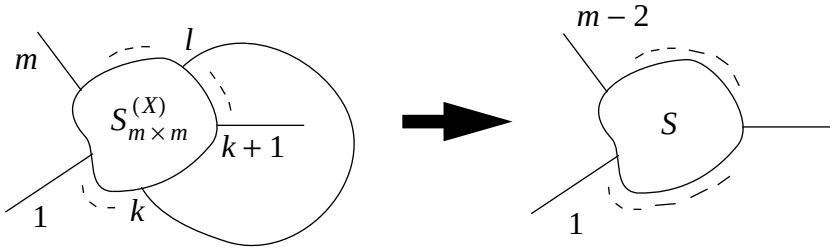

Figure 3: Self Merging.

has the following s-parameters:

$$S_{ji} = S_{ji}^{(X)} + S_{jl}^{(X)} a_l + S_{jk}^{(X)} a_k \qquad i, j = 1, 2, \ldots, m-2 \tag{2}$$

where

$$\begin{aligned} a_l &= \frac{1}{\Delta}\left(S_{li}^{(X)} S_{kk}^{(X)} + S_{ki}^{(X)}\left(1 - S_{lk}^{(X)}\right)\right) \\ a_k &= \frac{1}{\Delta}\left(S_{ki}^{(X)} S_{ll}^{(X)} + S_{li}^{(X)}\left(1 - S_{kl}^{(X)}\right)\right) \\ \Delta &= \left(1 - S_{lk}^{(X)}\right)\left(1 - S_{kl}^{(X)}\right) - S_{ll}^{(X)} S_{kk}^{(X)} \end{aligned} \tag{3}$$

The network reduction process begins with merging all internal components by repeatedly utilizing the Adjoined Merging rule for all internal nodes. The Self Merging rule is applied to eliminate all the self loops introduced by the Adjoined Merging process. Finally, a multi-port network characterized by its scattering parameters is derived.

The above reduction process does not require the network be an RC tree. Since we start with the s-parameter description of the system, which always exists for any physically realizable system, the formulation is completely general for any linear distributed-lumped network with scattering parameter descriptions. Another advantage is that the need for using lumped representation of transmission lines is eliminated since lossy transmission lines can be represented in the distributed form.

In order to speed up the network reduction process, the two types of series-operation are in-

will present an improved nonlinear driver model based on a current source model introduced in [6]. This new driver model is used in conjunction with the interconnect macro model. Computational procedures using MEF to analyze the combined models are provided in section 6 and experimental results are presented in the last section.

2 . Scattering Parameter Based Macromodel

Given an arbitrary linear network of distributed-lumped elements, a scattering parameter based macro model is introduced in [2]. The individual components in the network are described by their scattering parameters, and a systematic reduction algorithm is introduced to reduce the network with many internal nodes to a multiport macro model with user specifiable external sources and loads of interest, as shown in Figure 1.

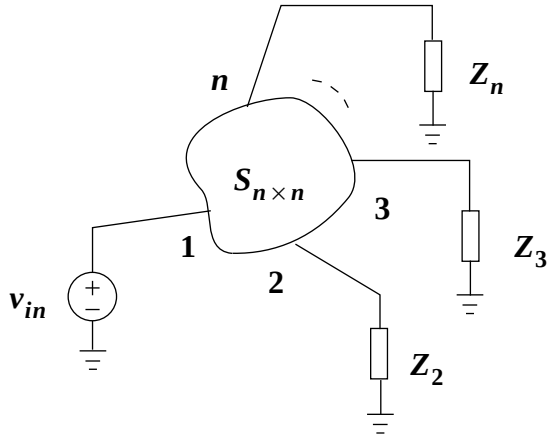

Figure 1: S-parameter based macromodel.

To obtain such a multiport representation with *n* external ports from an arbitrary distributed-lumped network of *m* original nodes, the network is reduced by merging the nodes into the multiport one at a time while keeping all user specified nodes external. There are two basic reduction rules:

Adjoined Merging Rule: Let *X* and *Y* be two adjoined multiports, with *m* ports and *n* ports respectively. Assume port *k* of *X* is connected to port *l* of *Y*, as shown in Figure 2. After merging *X*

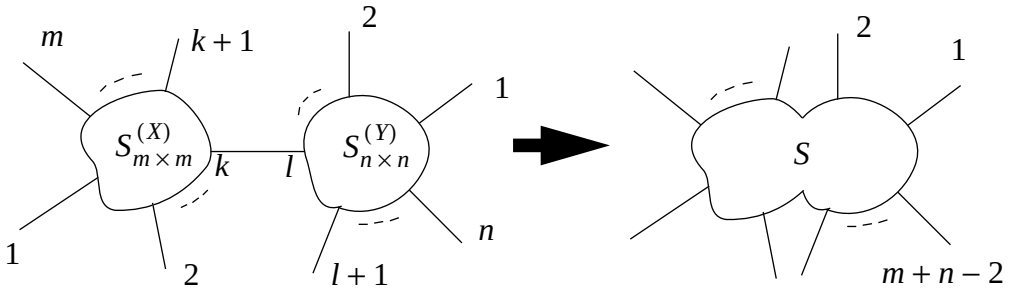

Figure 2: Adjoined Merging.

Transient Analysis of Interconnects with Nonlinear Driver Using Mixed Exponential Function Approximation

1 . Introduction

High speed interconnect networks have been studied quite extensively[1, 4, 5, 7] because of the ever increasing demand of high performance systems. Detailed analyses of interconnects are usually computationally expensive due to the distributed and dispersive nature of the network. The large number of internal nodes, which affect the external behavior of a network, adds to the complexity of the problem. However, the detailed inner working of these nodes are usually of little interests to the system designer and therefore, need not be explicitly represented into computational models. Similar to the idea of macro modeling the nonlinear gates to handle large designs, interconnect macro modeling is an attractive alternative. A scattering parameter-based macro model of distributed-lumped networks is introduced in [2]. That model handles general lumped and distributed elements as well as arbitrary network topologies. By representing only those nodes of interests as external ones, the size of the problem is significantly reduced.

Based on the scattering parameter macromodel, Pade technique can be used to approximate transfer functions of the interconnect system [2]. Pade approximation provides good accuracy with relatively little computation time, but may suffer from stability problem. In order to address stability problem, Exponentially Decayed Polynomial Function (EPDF) is used [3]. EPDF is guaranteed stable for a stable system, but it is computationally more expensive. In this paper, we present a new approximation function, called Mixed Exponential Function (MEF), that integrates the advantages of the two previously developed methods. It provides accuracy, efficiency, as well as stability.

Despite the increasing importance of interconnects in transient analysis, nonlinear active devices in a system also contribute to the system behavior significantly. However, most techniques geared towards interconnects tend to ignore the nonlinearity of the driving gates by the use of simple linear models for the drivers. With submicron CMOS design becoming common place, such linear driver models are no longer adequate. On the other extreme, detailed simulation device models are overly expensive for today's large systems. In sections 4 and 5 of this paper, we

Transient Analysis of Interconnects with Nonlinear Driver Using Mixed Exponential Function Approximation

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ABSTRACT

This paper presents a new technique that can efficiently and accurately evaluate the timing response of high speed interconnects, of which transient analysis becomes ever more important with the higher circuit speeds and finer feature sizes. This method is based on the scattering parameter macromodel, whose transfer function will be approximated by a new approximation function called Mixed Exponential Function (MEF). By taking advantage of the best properties of Pade approximation and Exponentially Decayed Polynomial function, this method efficiently achieves high accuracy afforded by the former, and high stability by the latter. A driver model suitable for sub-micron CMOS design is also presented to incorporate the nonlinearity of the circuit elements. The interconnect macro model and the nonlinear driver model combined with the Mixed Exponential Function approximation provide accuracy comparable to that of SPICE at a speed one to two orders of magnitude faster.

Keywords: scattering parameter, macromodel, multiport component, multiport interconnect node, component merging, network reduction, lossy transmission line, mixed exponential function, nonlinear driver, current source model, delay and Taylor series.

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1. with Cadence Design Systems, Inc.